STUDY OF PbSnTe SINGLE HETEROJUNCTION DIODES

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THESIS

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by

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ABSTRACT

The electrical and photovoltaic properties of single heterojunction (SH) $Pb_{1-x}Sn_xTe$ diodes have been studied. SH diodes were fabricated by sequential depositions of p-type $Pb_{0.86}Sn_{0.14}Te$ using stiochiometric source material and n-type $Pb_{0.80}Sn_{0.20}Te$ using metal rich source material. At T = 77°K, their energy gaps are 0.136 ev and 0.103 ev, respectively. SH diodes of good rectification with R_oA products ranging from 3.5 to 18.6 have been obtained. Operated at 100°K, 500°K black body photovoltaic responses up to 0.2 volt/watt has been obtained.

The current-voltage characteristics have been studied theoretically based on both the Anderson Diffusion Model and the Thermionic Emission Model. Using Anderson's model, and assuming $\Delta E_c = 0$, constant electron affinity across the junction, fair agreements have been found between measurements and theoretical calculations.

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LIST OF SYMBOLS

A - area

C - capacitance

D_p - hole diffusion constant

E_g - energy gap

E_{g1} - energy gap on n-side

E_{g2} - energy gap on p-side

ΔE_g - difference in energy gaps across the junction

ΔE_c - conduction band discontinuity

ΔE_v - valence band discontinuity

J - current density

J_o - saturation current

K - Boltzmann constant

N - carrier concentration

N_{A2} - hole concentration on p-side

N_{D1} - electron concentration on n-side

Q - electron charge

R_o - zero bias resistance

T - temperature in ^oK

V - applied voltage

V_{BE} - junction barrier to electron flow

V_{BH} - junction barrier to hole flow

V_D - junction barrier

X - fraction of holes with sufficient energy to cross the barrier which actually do cross

W - depletion layer width

ϵ - dielectric constant

ϵ_1 - dielectric constant on n-side

ϵ_2 - dielectric constant on p-side

η - deviation from ideal diode

τ_p - hole lifetime

ACKNOWLEDGEMENTS

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I would also like to extend special thanks to Mr. Ray Zahm for his laboratory supervision, for the deposition of films, and especially for his design of the multisource deposition chamber.

In addition, I would like to thank Capt. A. E. Romsos, my thesis partner, for his support and cooperation; Mrs. A. E. Romsos for typing the smooth rough, and M. Jaehnig for his assistance in the laboratory.

Finally, I would like to thank my wife and son for their understanding and support.

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I. INTRODUCTION

A. INTRODUCTION

The heterojunction semiconductor diode was first reported by R. L. Anderson in 1962.[1] His work was on the Ge - GaAs heterojunction. Since then, many other heterojunctions have been reported; including work by: Van Opdorp and Kanerva on Ge - Si [2]; Hinkley and Rediker on GaAs - InSb [3]; Donnelly and Milnes on Ge - GaAs [4]; and Dutton and Muller on CdS - CdTe [5]. Most recently, another heterojunction study was reported by J. Fernandez in a thesis at the Naval Postgraduate School on $Pb_{1-x}Sn_xTe$ [6]. This thesis is an extension of that work.

The term heterojunction is used to describe a semiconductor junction with different energy gaps on each side of the junction. In addition, the materials on either side of the junction usually have different electron affinities, fermi levels, dielectric constants, and doping concentrations. Heterojunction devices fall into one of two broad classifications: anisotype or isotype. The anisotype heterojunction has an n-layer on one side of the junction and a p-layer on the other side. The smaller of the energy gaps may be on either the n or the p side and may be in either the heavy or light doped layers. The isotype heterojunction has the same type majority carrier on each side, but with one side doped much higher than the other side; for example, $n - n^+$ or $p - p^+$.

This thesis will be concerned with the anisotype heterojunction. The n layer is $Pb_{0.80}Sn_{0.20}Te$ which has the smaller energy gap (E_{g1} = .103 ev) at 77°K. The p layer is $Pb_{0.86}Sn_{0.14}Te$ whose energy gap is 0.136 ev. at 77°K.

The $Pb_{1-x}Sn_xTe$ alloy semiconductor has been actively developed in recent years because of the unique property in that the energy gap can be made small by varying the alloy composition (varying x in $Pb_{1-x}Sn_xTe$). Consequently, PbSnTe has significant applications in the long wavelength infrared (LWIR) spectrum; specifically in the 8-14 micron atmospheric window. Until the recent work here at the Naval Postgraduate School, and possibly a few other laboratories like North American Science Center, Naval Ordinance Laboratory and Naval Research Laboratory, all the junction developments in PbSnTe have been homojunctions. Practical LWIR devices using PbSnTe have been very actively developed in the past two to three years.

It is the purpose of this thesis to continue research in the heterojunction already begun under the direction of Dr. T. F. Tao.

In conjunction with this thesis Capt. A. E. Romsos, U.S.M.C., has studied the photo response of the diodes. His results and work have been reported in another thesis which was completed in June 1973. The results of his work will be briefly mentioned in Part IV of this thesis.

B. PURPOSE OF THIS THESIS

1. Theory

The purpose of the theoretical portion of this thesis is:

a. Develop a band diagram for the anisotype single heterojunction $Pb_{1-x}Sn_xTe$ diode.

b. Calculate I-V characteristics.

c. Calculate C-V characteristics.

2. Experiment

The purpose of the experimental portion of this thesis is:

a. Manufacture anisotype single heterojunction PbSnTe diodes.

b. Justify proposed band diagram.

c. Measure their I-V characteristics and compare with theory.

d. Measure their C-V characteristics and compare with theory.

e. Measure their photovoltaic properties.

f. Identify further research required.

II. BACKGROUND

A. $Pb_{1-x}Sn_xTe$ NARROW GAP SEMICONDUCTOR

$Pb_{1-x}Sn_xTe$ is a pseudo-binary alloy with the B_1 rocksalt structure. Its energy gap depends on the composition, temperature, and pressure in a special way as explained by Dimmock et. al.[7], in the band inversion model. This model is shown in Figure 1. The variation of energy gap with composition is shown in Figure 2. Melngailis and Harman have reported experimental evidences to support this model [8].

By controlling the composition, temperature, and pressure the energy gap may be made as small as desired. Consequently, this semiconductor has important application in the long wavelength infrared atmospheric window (8-14 micron). Good single crystals can be produced, thus making it possible to fabricate infrared detectors as well as junction lasers.

In recent years, $Pb_{1-x}Sn_xTe$ has been developed with emphasis on the bulk crystals used in homojunctions.

The growth techniques include liquid epitaxy [9], Czochralski [10], open-tube vapor growth [11], closed-tube growth [12], and Bridgman [12].

$Pb_{1-x}Sn_xTe$ homojunction devices have been developed today both as detectors and lasers. Recently, J. Fernandez reported a $Pb_{1-x}Sn_xTe$ anisotype, thin film heterojunction [6].

J. Fernandez used the evaporation method to grow single crystal thin films on the cleaved (100) plane on KCL. Carrier concentration in his samples was in the low 10^{17} CM^{-3} range.

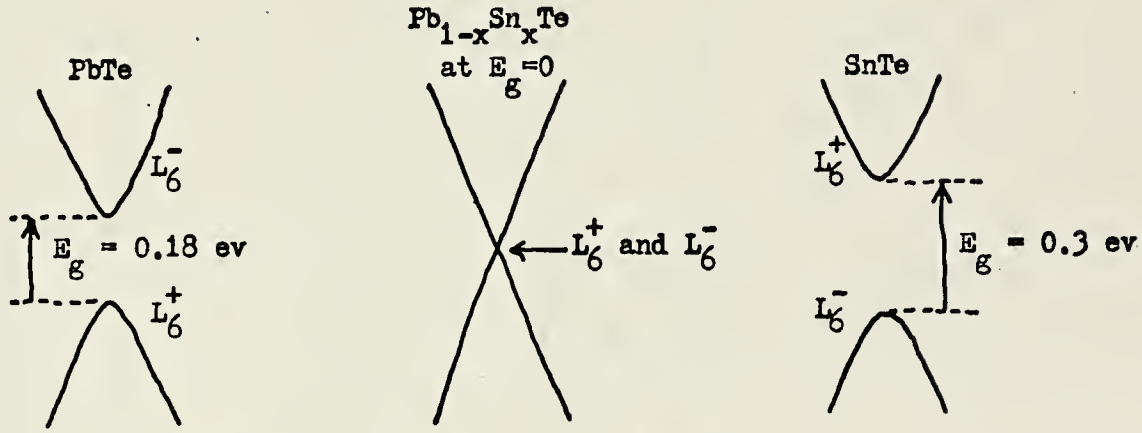

Figure 1. $Pb_{1-x}Sn_xTe$ Band Inversion Model

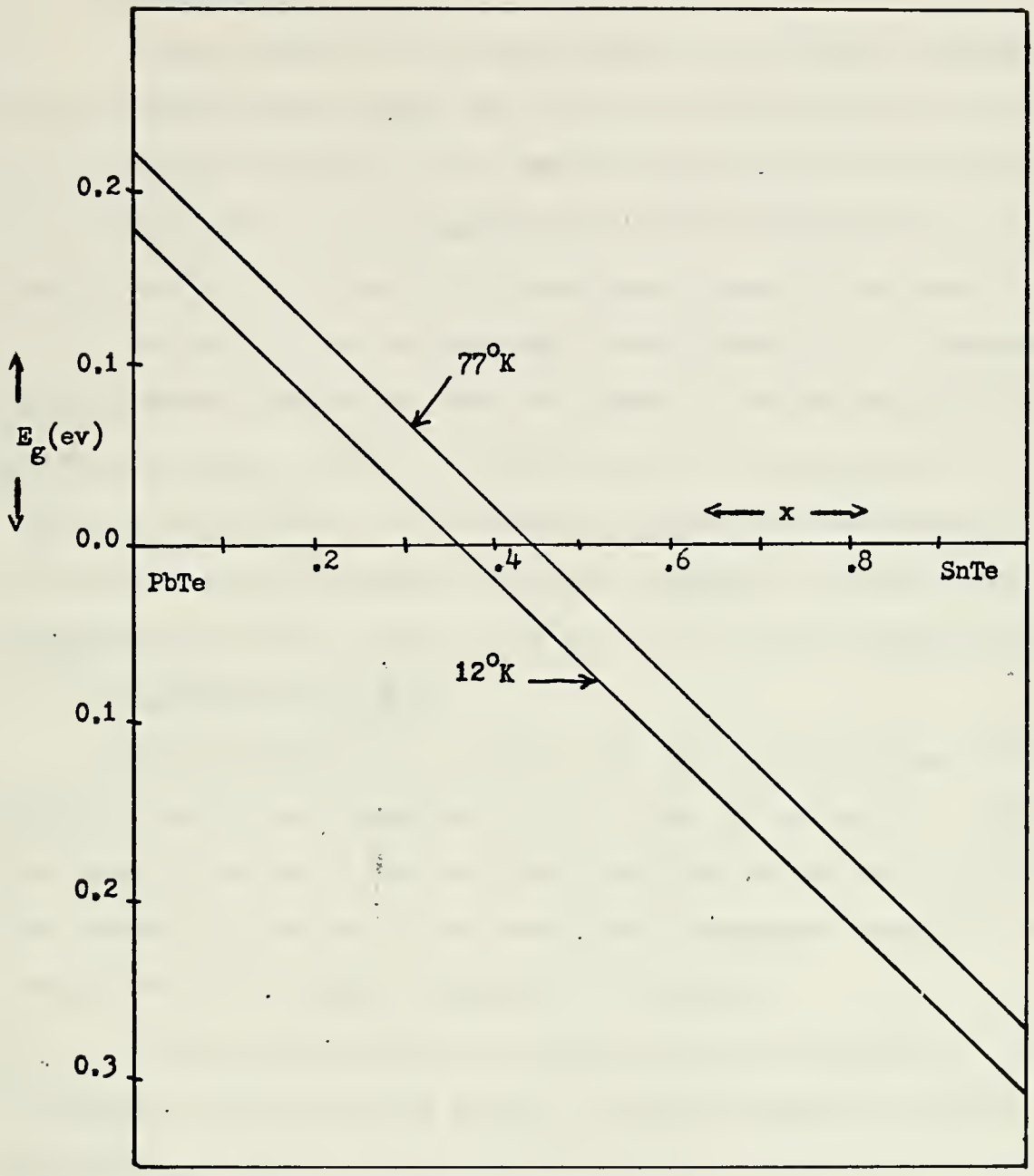

Figure 2. $Pb_{1-x}Sn_xTe$ Energy Gap Variation

B. HETEROJUNCTION DEVICES

1. Introduction

A heterojunction is a junction between two different semiconductors having different energy gaps. The first reported heterojunction was by R. L. Anderson in 1962 [1]. His junction was made between Ge and GaAs.

Since this work, a large number of other heterojunctions have been studied such as InP - GaAs, GaP - GaAs, InAs - GaAs, Ge - Si, etc.

In growing heterojunctions using two different III - V compound semiconductors, problems have been encountered in maintaining good crystal growth and having a minimum of interface states at the junction. To counter these problems, the alloy heterojunctions have been developed. They seem to have more promise for device application. Two outstanding examples are the GaAs - $GeAs_{1-x}P_x$ and GaAs - $Ga_{1-x}AL_xAs$ heterojunctions.

2. Band Diagram and Model

The homojunction is a junction with the same energy gap, electron affinity, and dielectric constant on both sides of the junction. Thus, the junction barrier to electron flow is the same as that to hole flow. The conduction bands and valence bands remain everywhere parallel to the vacuum level with a smooth transition at the junction.

In the heterojunction, the situation is more complicated. The difference in energy gaps and electron affinities across the junction cause discontinuities in either the conduction or valence bands or both. These discontinuities appear at the interface. In addition, the growth of two crystals of different lattice constants creates a transition region at the interface of dangling bonds. These dangling bonds create interface states and electric dipoles at the interface. The model for a heterojunction will depend on the material used to fabricate the

heterojunction. This model can be quite complicated. The model may be further complicated by tunneling and/or a generation-recombination mechanism.

Before describing a model and the theoretical calculation for $Pb_{1-x}Sn_xTe$ studied in this thesis, the work of others pertinent in developing the theoretical analysis in Part III will be reviewed.

The first theory of the anisotype n-p single heterojunction diode was proposed by R. L. Anderson in 1962 [1]. The simplified energy band diagram is shown in Figure 3. The figure is drawn for a large energy gap p side and small energy gap n side heterojunction diode (n-p heterojunction diode).

From the figure for the case of the n-p junction, the zero bias barrier to electrons, V_{BE} is:

$$V_{BE} = V_D + \Delta E_C$$

The zero bias barrier to holes, V_{BH} is:

$$V_{BH} = V_D - \Delta E_V$$

Additionally:

$$\Delta E_C + \Delta E_V = E_{g2} - E_{g1} = \Delta E_g$$

The barrier to hole flow is less than that to electron flow by ΔE_g. In the case of Ge - GaAs for which Anderson proposed the model, he then assumed that the hole current would dominate. From this, the equations for current density and junction capacitance are:

$$J = J_o(e^{QV/KT\gamma} - 1)$$

$$J_o = A\, e^{-QV_{BH}/KT}$$

$$A = XQ\, N_{A2}(D_p/\tau_p)^{\frac{1}{2}}$$

$$C = \left[\frac{Q\, N_{D1}\, N_{A2}\, \epsilon_1\, \epsilon_2}{2(\epsilon_1\, N_{D1} + \epsilon_2\, N_{A2})}\quad \frac{1}{V_D - V}\right]^{\frac{1}{2}}$$

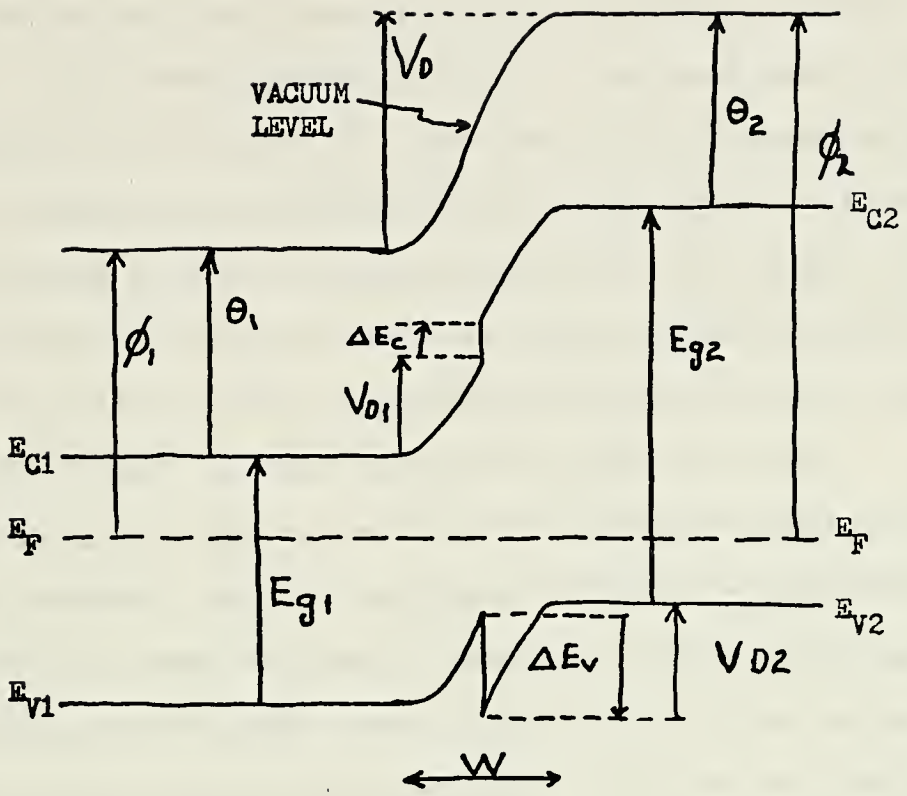

Figure 3. Anderson's n-p Model Band Diagram

Anderson's model is an extension of the ideal homojunction diode theory to include the difference in energy gaps. It represents a first order approximation and as such has served as the basis from which other researchers of the heterojunctions have started.

In 1966, Donnelly and Milnes reported their findings comparing Ge - Si and Ge - GaAs heterojunction [4], [13]. They found that Anderson's model was inaccurate for the Ge - Si. This was due to the interface state density at the junction and the electric dipole found across the junction. The lattice mismatch for Ge - Si is approximately 4% while for Ge - GaAs the lattice mismatch is 0.07%. Donnelly and Milnes reported that Anderson's model was valid as a first order approximation in the n-p Ge - GaAs. But, for p/n Ge - GaAs, a recombination-tunneling model was used.

The primary cause for the deviation from Anderson's model is that of the lattice mismatch. When two crystals of different lattice constants are grown together, a transition region exists which will contain dangling bonds. From these dangling bonds arise interface states which can act as either charge centers or recombination centers. Also, from the dangling bonds, electric dipoles can be formed across the junction. The effects of the interface state density and electric dipole on the current/voltage and capacitance characteristics are included in references [4] and [8]. When the lattice mismatch is small, the effects of these factors can be neglected (Anderson's Model).

Other deviations from Anderson's model include the effects of charge carriers tunneling across the junction via the interface states, charge carriers tunneling through the discontinuity spike in either the conduction band (electrons) or valence band (holes), the effects of deep interface state energy levels, thermionic emission, etc.

C. DEPOSITION OF FILMS

1. Introduction

J. Fernandez had some successes in growing single crystal $Pb_{1-x}Sn_xTe$ heterojunction diodes using the one boat evaporation method [6]. He was able to grow good quality, single crystal n and p layers with carrier concentrations in the low $10^{17}cm^{-3}$ range.

The carrier concentration and carrier type of $Pb_{1-x}Sn_xTe$ can be controlled by an isothermal annealing process. Both p and n type semiconductors can be obtained with carrier concentrations in the $10^{16}cm^{-3}$ range and on a few occasions as low as mid $10^{15}cm^{-3}$. This procedure does not lend itself well to the making of alloy heterojunction diodes where alloys of two different compositions are present.

J. Fernandez found that by using metal rich $(Pb_{1-x}Sn_x)_yTe$, n type thin film semiconductors could be made with carrier concentration in the low $10^{17}cm^{-3}$ range [6]. This is the method that will be continued in this thesis.

2. Preparation of Source Material

For the p layer, stiochiometric $Pb_{0.86}Sn_{0.14}Te$ alloy was used. For the n layer metal rich $(Pb_{0.80}Sn_{0.20})_yTe$ was used where y was greater than 1.0. Since excess PbSn acts as donors, by increasing the amount of PbSn, the semiconductor can be changed to n-type. Y has been varied from 1.002 to 1.030.

The source materials were made from 99.9999% pure Pb, Sn, and Te. Weighing was accurate to $\pm$ 0.0001 gram. The proportion of Pb, Sn, and Te was calculated using the following formulas:

$$Sn = 1.0$$

$$Pb = \frac{207.19}{118.69} \frac{(1 - x)}{(x)}$$

$$Te = \frac{127.60}{118.69\ xy}$$

After weighing, the values of x and y were checked using the following formulas:

$$X = \frac{207.19}{118.69\left(\frac{W\ Pb}{W\ Sn}\right) + 207.19}$$

$$Y = \frac{127.60}{118.69}\frac{(W\ Sn)}{(W\ Te)}$$

where the W indicates the actual weight in grams.

After weighing, the elements were vacuum sealed in quartz ampoules. They were then put in a furnace at 1150°C for 24 hours. After removal from the furnace, they were rapidly quenched in water in order to prevent excessive precipitation. The alloy ingots were then crushed into small pieces to be used in the evaporation boat.

Optical and Hall thin film samples were deposited on cleaved KCL substrates using the source material for the purpose of characterizing metallurgical, electrical and optical properties. The deposition procedure will be covered in the next section.

The metallurgical evaluation was performed to obtain information as to the thin film thickness, crystal structure, orientation, and composition. The thickness was obtained from the interference pattern in the transmission (or reflection) measurement using a Perkin - Elmer spectrophotometer. The crystal structure was determined using the x-ray laue picture technique. The orientation and composition were obtained with a Norelco x-ray diffractometer using a copper target.

It was found that consistent single crystal growth in the (100) orientation was obtained from growth as KCL substrates. The sample thicknesses varied from 2 - 8 microns.

The electrical properties were characterized using the Hall and conductivity measurements, to give the Hall coefficient, mobility,

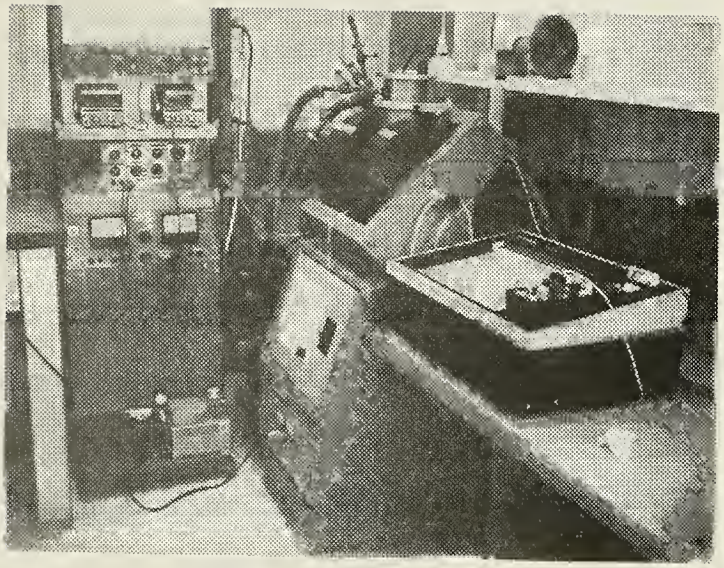

Figure 4. Hall Measurement Equipment

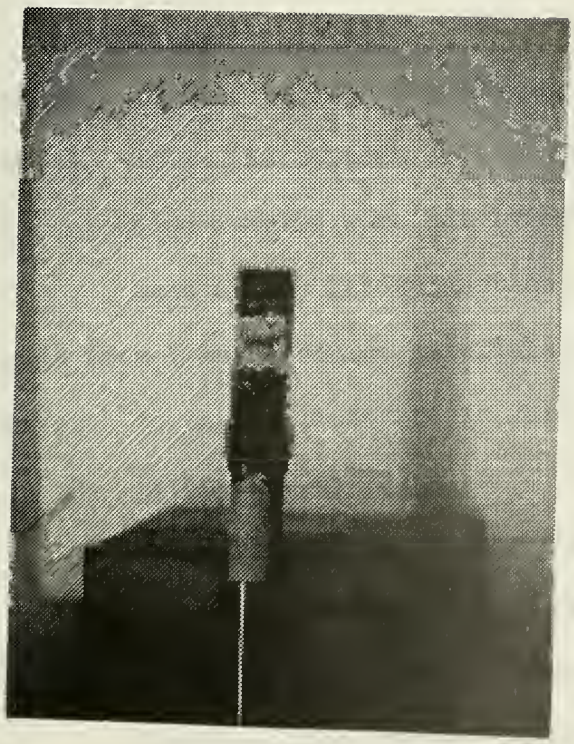

Figure 5. Hall Dewar Cold Finger

conductivity, carrier concentration, and carrier type. The Hall measurement setup is shown in Figure 4. The Hall measurements were carried out from 85°K to 300°K using liquid nitrogen to cool the samples. A 1 ma d.c. current was used. The electrical contacts were made by using silver epoxy to contact 3 mil copper wire to a gold pad deposited on the side arms of the Hall sample. It was found that by depositing gold pads before using the silver epoxy, smoother curves were obtained from the Hall measurements. The contacts were then mounted onto the cold finger using thermal conducting grease. The system was kept below 20 microns of vacuum during measurement. The cold finger used is shown in Figure 5.

Table I summarizes the results of electrical properties of thin films made from several different PbSn rich $Pb_{0.80}Sn_{0.20}Te$ source materials. Source materials A through H were made by J. Fernandez.

It should be noted that p type thin films were obtained using source materials C, E, F, G, and H. The reason for this is not understood. Since the purpose of this thesis is to study the heterojunction diode, these samples were not investigated any further.

Most of the heterojunctions made for study in this thesis were made from I and J source materials. Results from Hall measurements for several tests are presented in Tables II and III.

3. Deposition of Films

Two different deposition procedures were used during the course of this thesis. The first was a single source deposition chamber, the second, a multisource system. Both procedures will be described below.

In the single source procedure, a one-boat evaporation technique sometimes known as the Knudsen method is used. The material to be evaporated is placed in a closed graphite boat with a 1/16 inch diameter hole

TABLE I

SUMMARY OF SOURCE MATERIAL $(Pb_{1-x}Sn_x)_yTe$

SOURCE MATERIAL	X	Y	CARRIER TYPE	CARRIER CONC. ($1/cm^3$)	CONDUCTIVITY ($1/ohm-cm$)	MOBILITY ($cm^2/V-sec$)
A	0.2000	1.0047	N	MID 10^{17}	500	5000
B	0.1999	1.0028	N	LOW 10^{17}	300	4000
C	0.2000	1.0010	P	LOW 10^{18}	1400	8000
D	0.2000	1.0006	N	LOW 10^{17}	60	1500
E	0.2000	1.0020	P	HIGH 10^{17}	400	3000
F	0.2000	1.0030	P	LOW 10^{18}	200	1000
G	0.1999	1.0040	P	LOW 10^{18}	200	3000
H	0.2000	1.0060	P	LOW 10^{18}	900	3000
I	0.2000	1.0200	N	LOW 10^{17}	300-500	4000-10,000
J	0.2000	1.0299	N	MID 10^{17}	300	2000-10,000
L	0.2000	1.0149	N	LOW 10^{17}	80	2500
ST	0.1400	1.0000	P	MID 10^{17}	800	9000

TABLE II

SOURCE MATERIAL I HALL MEASUREMENTS

Sample	Carrier Concentration ($1/cm^3$)	Carrier Type	Mobility ($cm^2/V\text{-}sec$)
2 - 5	6.8×10^{16}	N	7235
1 - 5	4.5×10^{17}	N	10,302
1 - 2	4.0×10^{17}	N	9980
2 - 3	8.3×10^{16}	N	4764

TABLE III

SOURCE MATERIAL J HALL MEASUREMENTS

Sample	Carrier Concentration ($1/cm^3$)	Carrier Type	Mobility ($cm^2/V\text{-}sec$)
5 - 2	2.3×10^{17}	N	4523
5 - 3	2.3×10^{17}	N	9239
5 - 5	2.8×10^{17}	N	2297

in the top cap. The boat is then placed inside a tungsten basket heater, as shown in Figure 6.

Next KCL crystals are cleaved to a thickness of about 1/8 inch and mounted in the substrate holder shown in Figure 7. The masks installed in the substrate holder permit growing of both optical and Hall samples. The two masks are shown in Figures 8 and 9. Usually two optical samples and four Hall samples were made during each deposition. The seventh position was used for a thermocouple to moniter the substrate temperature. The substrate holder was then placed in position over the chamber. The substrate heater was placed over the substrate holder. The arrangement is shown in Figures 10 and 11.

A shutter was then placed between the substrate and the boat. The boat was shielded inside a molybdenum enclosure to decrease heat losses.

With the equipment in position the bell jar was lowered and the chamber evacuated to 10^{-6} torr vacuum. The substrate heater was then turned on. Substrate temperatures of 240°C - 270°C were used. The tungsten basket heater was then turned on and the boat was heated to between 650°C-760°C. Once the boat was at the proper evaporation temperature, evaporation onto the shutter was done for about 5 minutes allowing the initial sublimations to be deposited on the shutter. The shutter was then swung out of the chamber and evaporation onto the substrate began. The length of time of deposition was determined by the desired thickness. This also varied with the boat and substrate temperatures employed. Table IV presents data on some of the depositions made.

After the desired evaporation time, the shutter was returned into the chamber between the substrate holder and the boat. The boat heater

Figure 6. Single Source Basket Heater

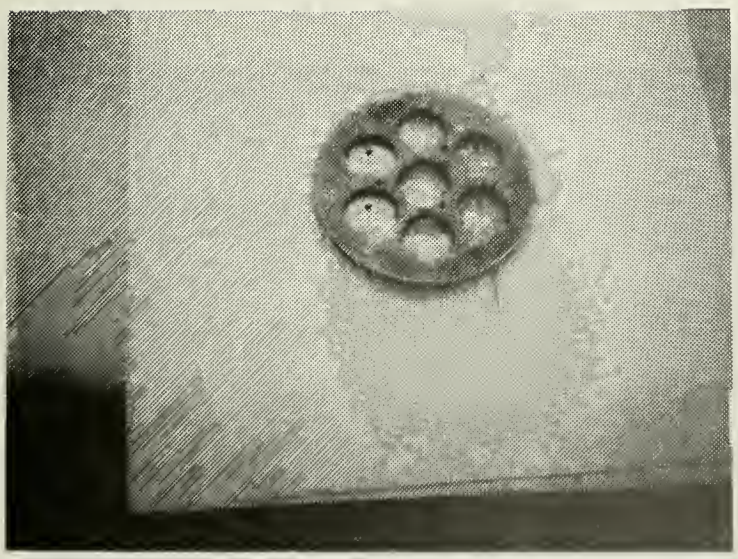

Figure 7. Substrate Holder

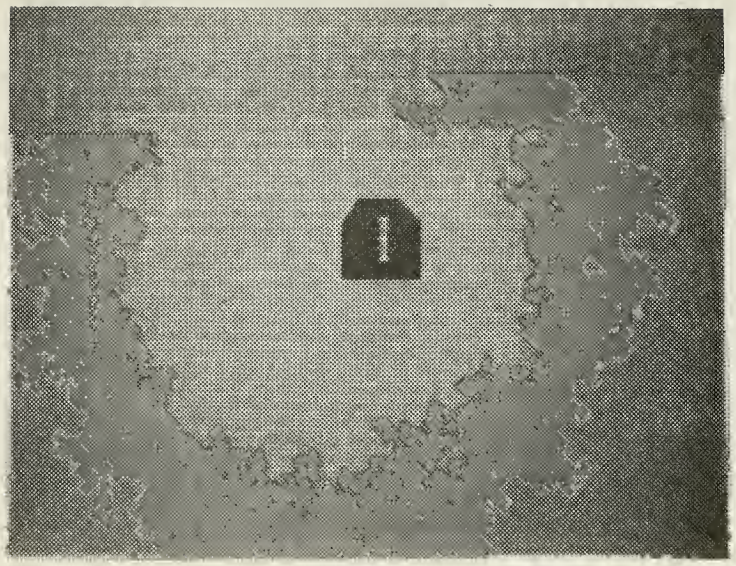

Figure 8. Hall Sample Mask

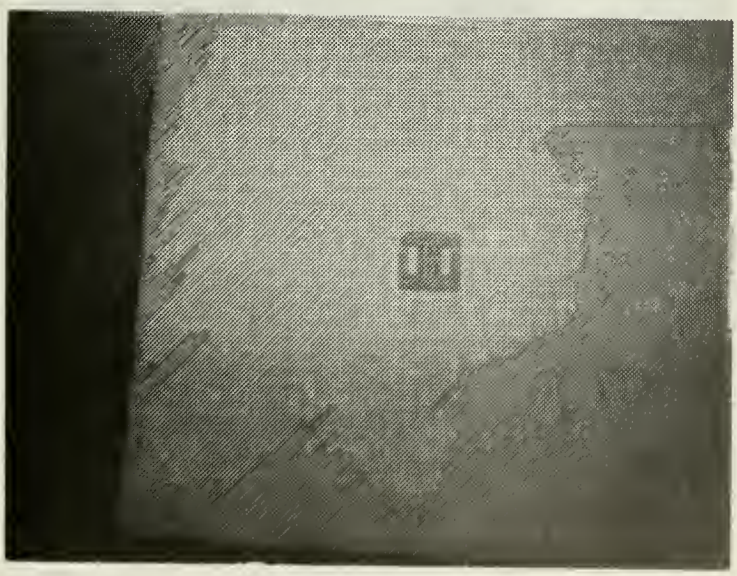

Figure 9. Optical Sample Mask

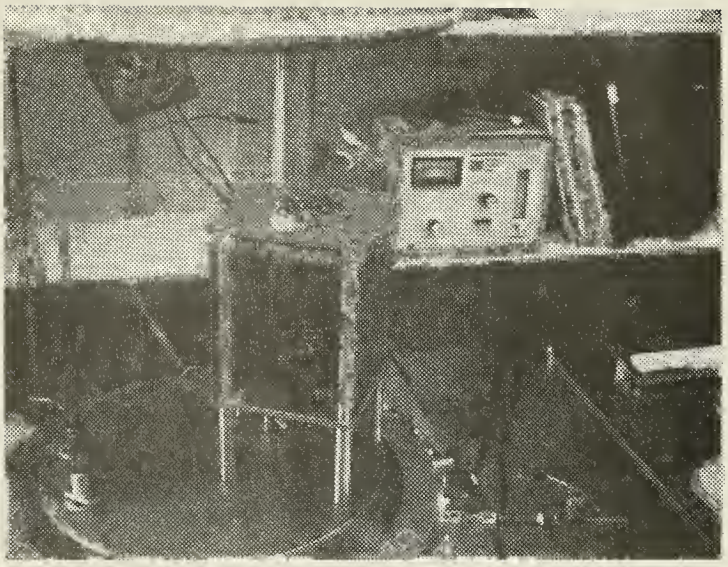

Figure 10. Substrate Holder in Position

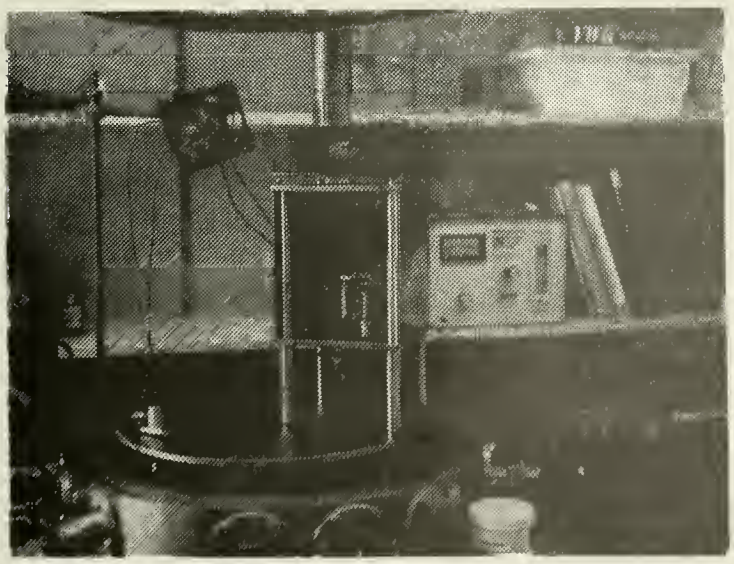

Figure 11. Substrate Heater in Position

TABLE IV

TYPICAL SINGLE SOURCE DEPOSITIONS

Sample	Source Material	Boat Temperature (°C)	Substrate Temperature (°C)	Time (min)	Thickness (microns)
ST-20-SR-B-1	B	700	250	40	2.7
ST-20-SR-I-1	I	750	270	60	9.0
ST-20-SR-J-1	J	680	300	60	1.9
ST-20-SR-L-1	L	680	280	45	2.4
ST-20-SR-I-3	I	710	290	60	2.1
ST-20-SR-J-3	J	660	290	60	1.0

and the substrate heater were turned off. A period of about 6 hours was allowed for cooling. Normal pressure was then restored in the chamber. The samples could then be removed.

If Hall and optical samples were being made for metallurgical and electrical characterization, only one deposition was necessary. When heterojunctions were made, two depositions were required. After the first deposition, the system was opened. The boat was changed to one containing the material for the other layer. Usually the n layer was evaporated first followed by the p layer. Next the four Hall samples were removed from the substrate holder and four new pieces of KCL crystals installed. The two optical samples remained in place. The second layer was grown on top of the layer already on the optical samples forming the heterojunction diodes. With the changes made, the deposition process was repeated. The length of time the system was exposed to the atmosphere for the changes and pump down was normally about 25 minutes. This means that the interface between the two layers in the heterojunction was exposed to the atmosphere for this period of time. The effects of this exposure will be discussed in Part IV.

In order to eliminate exposure of the interface to the atmosphere, Mr. Ray Zahm designed a multisource deposition unit. In this design, shown in Figure 12, two deposition chambers are used. One for the n type layer and one for the p type layer. The loading of the boats in each chamber is identical to the single source deposition unit. The substrate holder is only loaded once in the multisource system. Moniter Hall samples for deposition of each layer cannot be made. The substrate holder is then placed in position on the rotatable top platform. The substrate heater is placed over the substrate holder. The chambers are enclosed in

a quartz tube to prevent the vapor from spreading all over the vacuum system. The assembled system is shown in Figure 13. The bell jar is then lowered and the system is evacuated to a vacuum of 10^{-6} torr.

The substrate is then rotated to a vacant chamber, see Figure 14. This places a shield (the top plateform) over the chamber to be used first. The substrate heater and the boat heater are then heated to the desired temperatures. Initial evaporation onto the top plateform is allowed for 5 minutes to capture the initial deposits. The substrate holder is then rotated to the chamber for evaporation of the first layer.

This is shown in Figure 15. When the desired evaporation time has been reached, the substrated holder is again rotated to a vacant chamber as shown in Figure 14. The boat heater in the first chamber is turned off and the heater in the second chamber is brought up to temperature. Once up to the desired temperature, evaporation onto the top plate is allowed for 5 minutes. The substrate holder is then rotated into position over this chamber for deposition of the second layer, see Figure 16. Note that Figures 14, 15, and 16 were taken with the bell jar raised. When in operation the bell jar would remain down throughout the deposition.

When deposition was completed, the substrate holder was again rotated to a vacant chamber. The substrate heater and boat heaters were turned off. A period of 6 hours was allowed for cooling before removing the samples.

The advantage of this system over the single source system is in the fact that the entire deposition procedure is carried out under vacuum of 10^{-6} torr. As will be discussed in Part IV, better heterojunctions seem to have been made in the multisource system.

A disadvantage in the multisource system as presently utilized is the absence of monitor Hall samples for each deposition. However, it has

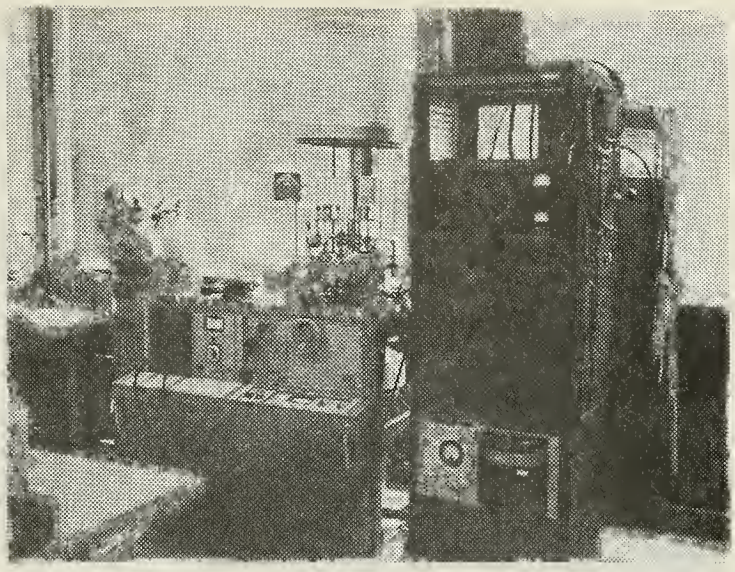

Figure 12. Multisource Deposition System

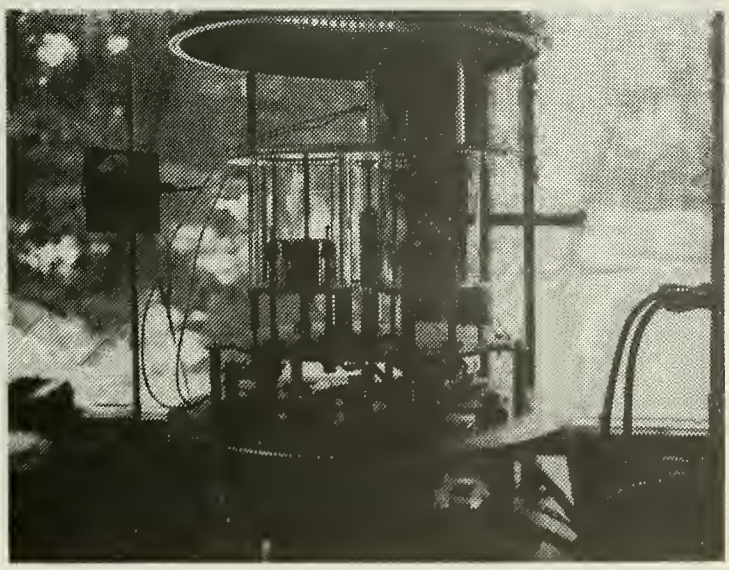

Figure 13. Assembled Multisource System

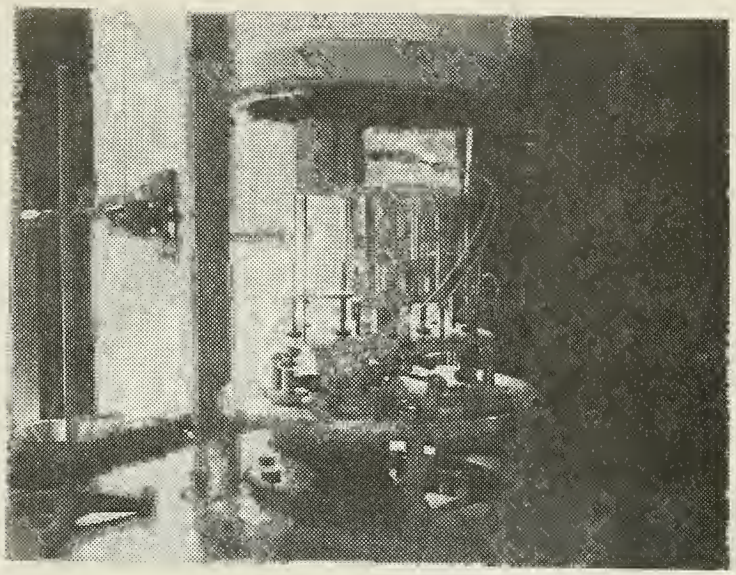

Figure 14. Substrate Over Vacant Chamber

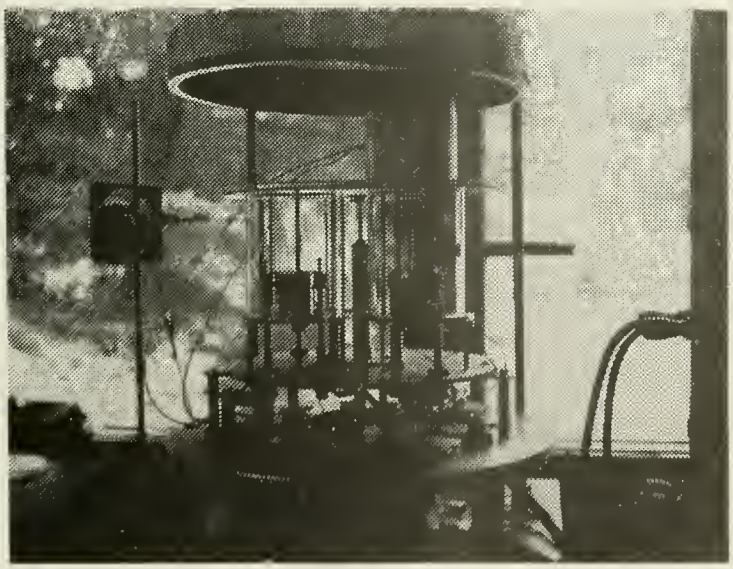

Figure 15. Substrate in Position for First Deposition

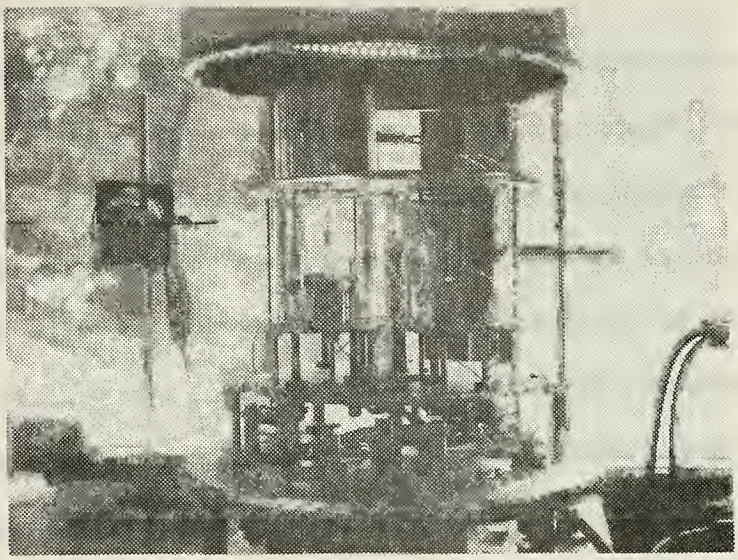

Figure 16. Substrate in Position for Second Deposition

been found in this study and also reported in reference [6] that for a given source material when evaporation parameters (substrate temperature, boat temperature, deposition time, type substrate) are held constant, the films grown have very similiar electrical and metallurgical characteristics. This fact decreases the need for monitor samples. Before making any heterojunctions in the multisource system, simple layer films of Hall and optical samples were first grown in test depositions for preliminary characterization. The evaporation parameters used in these test depositions were repeated during the making of the heterojunction. The time of deposition was varied to yield the desired thickness. The thickness of each layer can only be estimated from known heater temperatures and deposition times. Table V presents data on some of the single film depositions made in the multisource system.

After deposition of the films a thin (5000 Å) layer of gold was deposited onto the heterojunction.

4. Quality of Films

The thin films grown in both the single and multisource systems showed good adherence to the KCL substrate. Their thickness varied from 1-10 microns. Single crystal growth was consistently obtained.

KCL substrates were used for the following reasons: a) good adherence of thin films, b) (100) crystal orientation, c) dissolubility in water, d) ease of cleaving, and e) consistent single crystal thin films. The KCL crystals used had a high density of cleavage steps which were manifest in the thin films. One problem possibly due to these cleavage steps was encountered when the thin film first grown on the substrate was quite thin, less than 2 microns, and then a thick layer of 6 microns in the next layer. When the KCL substrate was dissolved away and gold deposition was attempted onto the first layer, the diodes were consistently

TABLE V

SINGLE FILM MULTISOURCE DEPOSITION

Sample	Source Material	Boat Temperature (°C)	Substrate Temperature (°C)	Time (min)	Thickness (microns)
ST-20-SR-J-4	J	690	280	30	1.9
ST-14-SR-1	ST	680	280	120	5.5
ST-20-SR-L-2	L	680	280	120	5.9
ST-20-SR-J-5	J	680	280	60	3.4
ST-20-SR-J-4	J	680	280	30	1.9

short circuits. It is believed that at the cleavage steps the gold may have diffused through the junction as the thickness of the layer at these cleavage steps may be very thin. It is most likely that the cleavage steps in the diodes have adversely effected the diode characteristics. The degree of this effect has not been examined as no attempt was made to remove any of the cleavage steps.

III. THEORETICAL STUDY OF $Pb_{1-x}Sn_xTe$ HETEROJUNCTION DIODES

A. INTRODUCTION

$Pb_{1-x}Sn_xTe$ material technology has not been advanced to the stage of elimination of material problems. The mechanism of conduction and the origin of charge carriers is not completely understood. As such, many inconsistencies are encountered. The location of impurity energy levels within the energy gap is not known. The preparation of thin film $Pb_{1-x}Sn_xTe$ heterojunction diodes is a completely new procedure. Whenever thin film devices are made, material difficulties are more pronounced. Because of the newness of this work and the material problems known to exist, the theoretical model developed will at best be a first order approximation to $Pb_{1-x}Sn_xTe$ heterojunction diode behavior. This theoretical model is very helpful in research to provide a guide in the evaluation of fabricated diodes. As $Pb_{1-x}Sn_xTe$ heterojunction research is continued, the first order approximation can be improved and refined.

B. THEORETICAL DIFFUSION MODEL

In selecting a model to be used for the $Pb_{1-x}Sn_xTe$, the first consideration must be the amount of lattice mismatch at the interface. Donnelly and Milnes have reported that Anderson's model is a good first order approximation for Ge-GaAs with 0.07% lattice mismatch but not for Ge-Si with a 4% mismatch [13].

Bis and Dixon have reported that for small deviations from stiochiometry Vegard's Law applies. This law states that the lattice constant of an alloy is linearly dependent on the mole fraction ratio in the alloy [14]. The lattice constant for SnTe is 6.327 Å and for PbTe is 6.460 Å

[14]. The largest deviation from stiochiometry in the metal rich materials is 3%. The lattice constant for the n type layer, of x = 0.20, is then calculated to be 6.346 Å and for the p type layer, of x = 0.14, 6.354 Å. The lattice mismatch is then 0.126%. This is larger than for Ge-GaAs but significantly smaller than for Ge-Si. Since interface states find their origins in dangling bonds created by lattice mismatch, and since the $Pb_{1-x}Sn_xTe$ heterojunction diodes studied here display a lattice mismatch on the order of Ge-GaAs, it is assumed the interface state density can be ignored. Furthermore, there are evidences indicating that the electrical properties of 4-6 compound and alloy semiconductors are not affected by lattice defects at the surface as in other semiconductors. A most convincing support of this fact is the success of fabricating Schottky barrier $Pb_{1-x}Sn_xTe$ diode laser which indicated that the surface layer of $Pb_{1-x}Sn_xTe$ is still of high enough quality to permit efficient luminescence and lasing [7]. It is also assumed that tunneling does not occur across the junction via interface states.

Since the materials on each side are different only by 6% mole fraction ratio (x = 0.14 for the p type and x = 0.20 for the n type), it is assumed both sides of the junction have the same dielectric constant (400) and the same electron affinity. There has been some evidence that the dielectric constant may be smaller. The assumption of the constant electron affinity across the junction is significant in the structure of the energy band diagram. The electron affinity represents the energy required to lift an electron from the bottom of the conduction band to the vacuum level. The conduction and valence bands are always parallel to the vacuum level. Thus all the discontinuity at the junction will appear in the valence band. ΔE_c is equal to zero.

To complete the energy band diagram one more assumption is made. At carrier concentrations of low 10^{17} cm^{-3} $Pb_{1-x}Sn_xTe$ becomes degenerate. It is assumed that the fermi level is located at the bottom of the conduction band on the n side and at the top of the valence band on the p side. From this assumption V_D will be equal to the energy gap on the p-side.

The simplified energy band diagram proposed for this thesis is shown in Figure 17.

From the geometry of Figure 17 and the assumptions made the following calculations can be made:

$$\Delta E_g = E_{g2} - E_{g1} = 0.033 \text{ ev}$$

$$\Delta E_c + \Delta E_v = 0.033 \text{ ev}$$

$$\Delta E_c = 0$$

therefore:

$$\Delta E_v = 0.033 \text{ ev}$$

$$V_D = E_{g2} = 0.136 \text{ ev}$$

$$V_{BE} = V_D = 0.136 \text{ ev}$$

$$V_{BH} = V_D - \Delta E_V = 0.103 \text{ ev}$$

From Anderson's paper the current density can be calculated using the following formulas [1]:

$$J = J_o \left(e^{QV/\gamma KT} - 1\right)$$

$$J_o = A\, e^{-QV_{BH}/KT}$$

$$A = X\, Q\, N_{A2} \left(D_p / \tau_p\right)^{\frac{1}{2}}$$

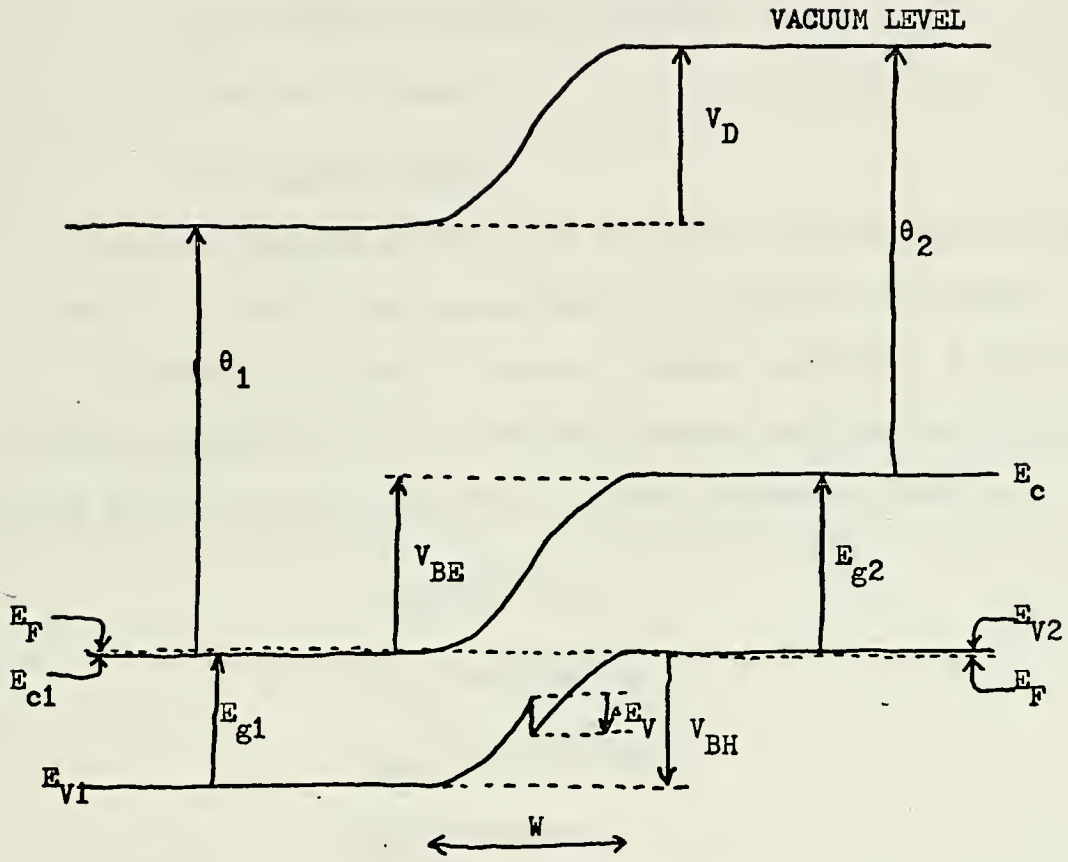

Figure 17. Theoretical Diffusion Model
Simplified Energy Band Diagram

where:

X = the fraction of carriers with sufficient energy to cross the barrier which actually cross the barrier

N_{A2} = hole concentration on the p-side

V_{BH} = hole barrier

η = deviation from the idea diode

D_p = diffusion constant for holes

τ_p = hole lifetime

V = applied voltage

Since the barrier to hole flow is less than the barrier to electron flow by 0.033 ev, it is assumed that hole current will dominate.

To compute J_o, X must be known. Anderson calculated X from experimental measurements of J_o. The same approach will be used in this thesis. This will be discussed in Part IV. Other parameters used are:

$$\tau_p = 10^{-9} \text{ sec}$$

$$D_p = 66.4 \text{ cm}^2/\text{sec}$$

$$N_{A2} = 5 \times 10^{17} \text{ cm}^{-3}$$

$$V_{BH} = 0.103 \text{ ev}$$

The capacitance and junction width formulas from Anderson is given as [1]:

$$C = \left[\frac{Q\, N_{D1}\, N_{A2}\, \epsilon_1\, \epsilon_2}{2(\epsilon_1\, N_{D1} + \epsilon_2\, N_{A2})} \qquad \frac{1}{(V_D - V)}\right]^{\frac{1}{2}}$$

$$W = \left[\frac{2\, \epsilon_1\, \epsilon_2 (V_D - V)\, (N_{A2} + N_{D1})^2}{Q(\epsilon_1\, N_{D1} + \epsilon_2\, N_{D2})\, N_{D1}\, N_{A2}}\right]^{\frac{1}{2}}$$

where:

N_{A2} = hole concentration on the p-side

N_{D1} = electron concentration on the n-side

ϵ_1 = dielectric constant on the n-side

ϵ_2 = dielectric constant on the p-side

V_D = barrier voltage

The junctions studied in this thesis have approximately the same carrier concentration on both sides of the junction. Anderson's equations for capacitance and junction width simplify to:

$$C = \left[\frac{Q\,N\,\epsilon}{4(V_D - V)}\right]^{\frac{1}{2}}$$

$$W = \left[\frac{4\epsilon(V_D - V)}{Q\,N}\right]^{\frac{1}{2}}$$

Plotting $1/C^2$ versus V the junction can be further analyzed. If the $1/C^2$ versus V is a straight line, then the junction is abrupt. The intercept of this curve on the voltage axis occurs at approximately V_D. The slope can be used to evaluate the carrier concentration using the following formula:

$$N = \frac{4}{Q\epsilon\left(\frac{d\ 1/C^2}{d\ V}\right)}$$

One of the purposes of the experimental portion of this thesis will be to validate the use of the above model. This will be done in the following steps:

1) Check for exponential relationship in the I-V curve.

2) Check for 1/T vs ln I dependence.

3) Measure V_{BH} from I-V and V_D from C-V measurements.

4) Compare magnitudes of measured I-V and C-V characteristics with the theoretical calculations.

A computer program has been developed to analyze both I-V and C-V data. These programs are included at the end of the thesis.

C. THERMIONIC EMISSION MODEL

In the Thermionic Emission Model, the capacitance calculations are the same as for the Diffusion Model. The current calculation is different.

The Thermionic Emission Model for a heterojunction is presented by SZE in reference [15]. The current density is given by the following formulas:

$$J = J_o \left(1 - \frac{V}{V_D}\right) \left(e^{QV/\eta KT} - 1\right)$$

$$J_o = \frac{QA^* TV_D}{K} e^{-QV_D/KT}$$

$$A^* = \frac{4\pi QM_e^* K^2}{h^3}$$

where:

A^* = Richardson's Constant

V_D = barrier voltage

M_e^* = electron effective mass

V = applied voltage

h = Planck's Constant

η = deviation from the ideal diode

For $Pb_{1-x}Sn_xTe$ A^* was calculated to be 2.3987. Assuming V_D = 0.136 ev J_o was calculated to be 3.7216×10^{-4} amp $\cdot$ cm^{-2}.

The barrier to hole flow is smaller than the barrier to electron flow. If it is assumed that hole current dominates, and V_{BH}, the barrier to hole current, is used in place of V_D then $J_o = 4.0552 \times 10^{-2}$ amps $\cdot$ cm^{-2}. V_{BH} was assumed to be 0.103 ev.

A study of the references applicable to this thesis indicates a strong preference for the Diffusion Model over the Thermionic Emission Model for heterojunctions. Also, in private communication with Mr. R. B. Schooler of Naval Ordinance Laboratory, a preference for the Diffusion Model was concluded. In work with PbTe diodes, Mr. Schooler has found that the Diffusion Model gave good agreements.

IV. EXPERIMENTAL RESULTS

A. FABRICATION OF SINGLE HETEROJUNCTION $Pb_{1-x}Sn_xTe$ DIODES

After depositions of the films and gold layer, the sample was cleaved into small pieces for mounting on TO-5 headers. The area of the diodes varied from $1 \times 10^{-3} cm^2$ to $4 \times 10^{-2} cm^2$. After cleaving, the small piece was mounted on the header using silver epoxy. When the epoxy was dry, the KCL was dissolved using deionized water. After the TO-5 header dried, a 1 mil copper wire was connected from the top of the thin film to the post of the header. In some instances, two wires were connected from different points on the sample to separate posts. This, in addition to providing two measurement points across the same diode, permitted an evaluation of the ohmic nature of the contact made by the epoxy to the thin film. Whether the p layer was on top depended on which layer was deposited first.

Care must be taken in the mounting to avoid an overflow of the silver epoxy at the edge of the sample. The use of a microscope in the fabrication of the diodes made working easier.

The geometry of diode construction is depicted in Figure 18. Four series of $Pb_{1-x}Sn_xTe$ diodes were fabricated from 14% stiochiometric p-type material and 20% metal-rich J or I material. Identification of layers for each series as well as deposition conditions is included in Table VI. A-Series was fabricated in the single source system and monitor samples were available from which the thickness could be measured. The remaining series were made in the multisource system. Monitor samples were not available to measure the thickness of each layer. The thickness was estimated from the knowledge of deposition conditions. A discussion of each series follows:

NOTE: Figure not drawn to scale.

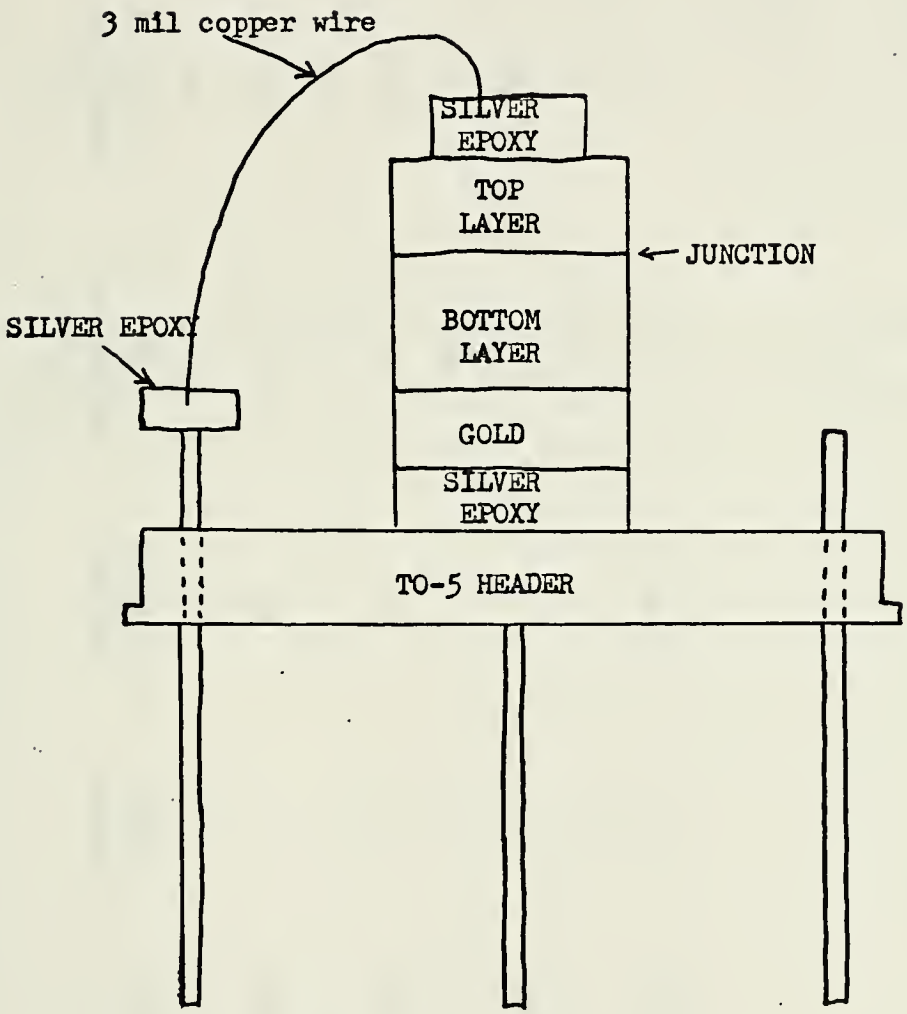

Figure 18. Diode Construction

TABLE VI

SUMMARY OF HETEROJUNCTION DEPOSITION

Series	Layer	Carrier Type	Source Material	Substrate Temperature (°C)	Boat Temperature (°C)	Deposition Time (min)	Thickness (microns)
A	TOP	N	J	280	680	45	1.9
	BOTTOM	P	ST	280	700	120	5.6
C	TOP	N	J	280	690	30	2
	BOTTOM	P	ST	280	680	120	6
D	TOP	P	ST	280	680	30	2
	BOTTOM	N	I	280	690	120	6
E	TOP	N	I	270	750	40	6
	BOTTOM	P	ST	270	750	40	6

1. A-Series

This series was made in the single source system. The junction interface was exposed to the atmosphere for about 45 minutes.

When these diodes were tested on the curve tracer, no rectification occurred until they had been subjected to a high voltage. Until this high voltage had been applied, the diode behaved as a very high resistance. They often approached an open circuit. The amount of voltage required to form the diode varied from 2 - 20 volts. As the voltage was increased on the curve tracer to form the diode, the I-V characteristic would suddenly change to a rectification curve when the forming voltage was reached. Once the diode was rectifying, high voltages would burn it out. If the diodes were then set idle for a few days, they usually required this high forming voltage again to obtain rectification.

The current through these single heterojunction diodes was lower than expected from theoretical calculations based on the theoretical model. A sample I-V curve is shown in Figure 19.

The "forming" behavior of these diodes was explained by the presence of a blocking oxide layer which was formed at the junction during exposure to the atmosphere. The high voltage required to turn on the diode was then smaller than expected because only the burned out area was conducting and this was much smaller than the actual physical area of the diode. It was then reasoned that the diodes had to be grown under a completely closed system. It was at this point in the study that Mr. Ray Zahm designed the multisource system.

If the explanation of the diode behavior is correct, it may be feasible to manufacture a metal-insulator-semiconductor. Oxidation should be faster at higher temperatures. If the system was opened to the atmosphere at temperatures higher than room temperature and left open, it may

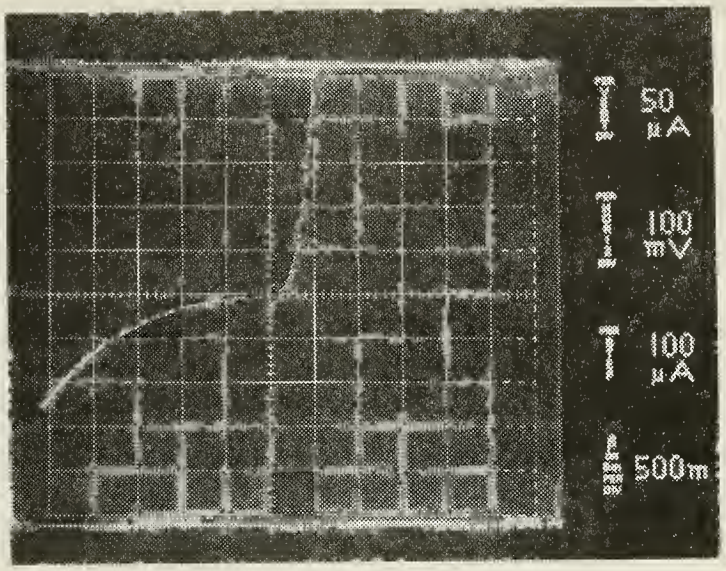

Figure 19. A-Series Diode

be possible to form an insulating layer on which metal could be deposited forming an MIS device. This idea has not been further investigated.

2. C-Series

This series was made in the multisource system. When these diodes were tested on the curve tracer, no voltage was needed. In fact, the diodes could be easily burned out with voltages across the diode of less than 200 mv. Photovoltaic response to a 300 watt light bulb was obtained. None was obtained to a 500°K blackbody [16]. A sample I-V curve is shown in Figure 20. The current will be compared with a theoretical analysis in the next section.

3. D-Series

To try and improve the photovoltaic response the p-type layer (larger energy gap) was placed on top to utilize the window effect.

The diode behavior was similar to the C-Series diodes except that better photovoltaic response was obtained. Photovoltaic response to a 500°K blackbody was obtained [16]. A sample I-V curve is shown in Figure 21.

4. E-Series

Both the C and D series diodes were found to rapidly deteriorate. In 12 - 24 hours the diodes would cease to rectify. As they deteriorated, their resistance approached an open circuit. They could not be restored by applying forming voltage. E-series was made with both layers over 5 microns thick to see if the deterioration was caused by interaction of top layers with atmosphere. This deterioration was not observed in the A-series diodes.

The diode performance was similar to the D-series. The photovoltaic response to a 500°K blackbody was less than for the D-series [16].

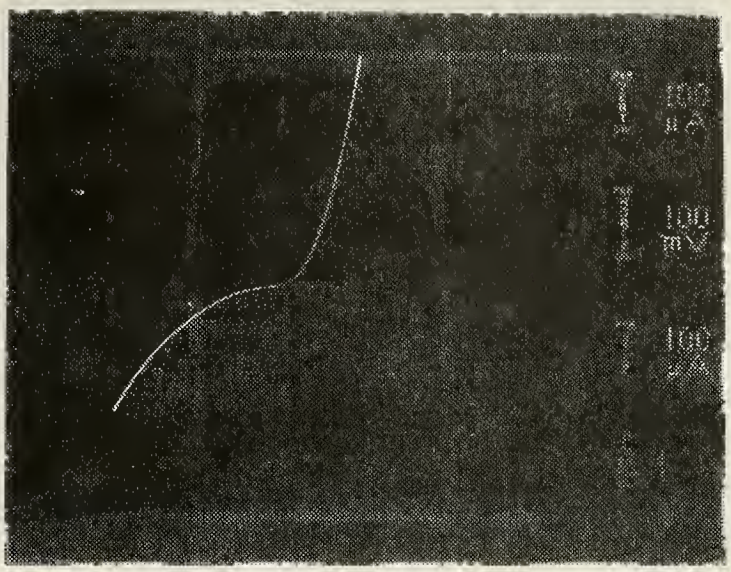

Figure 20. C-Series Diode

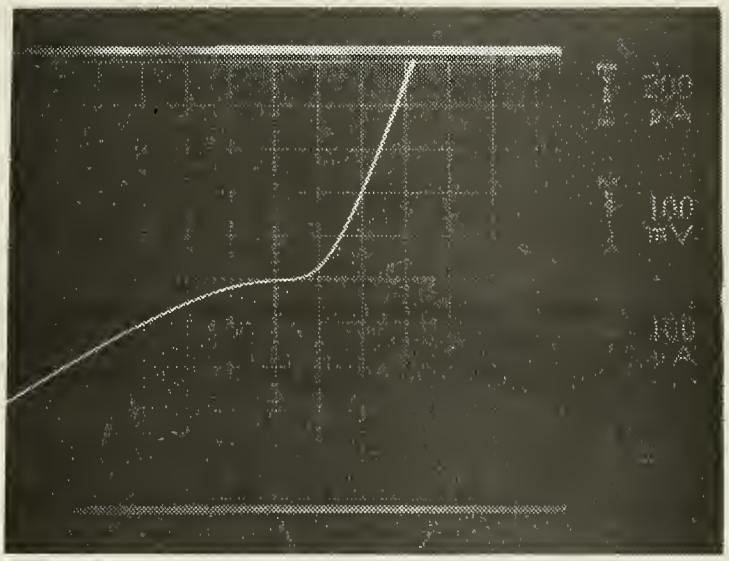

Figure 21. D-Series Diode

These diodes did not deteriorate as did the C and D series. I-V curves of two samples are shown in Figures 22 and 23. Figure 22 is typical and Figure 23 was the best diode obtained.

B. CURRENT - VOLTAGE ANALYSIS

The forward current - voltage characteristics for several diodes are presented in Figures 24 through 28. The pertinent data from these diodes is summarized in Table VII. The theoretical curve shown in the figures was computed using Anderson's Diffusion Model. The diode curves are presented with the voltage drop across the series resistance removed.

In the formula for computing J_o, X, the fraction of carriers with sufficient energy to cross the barrier which actually do cross the barrier, was computed from the measured J_o. This is presented in Table VII. The theoretical curve computation utilizes an average X of 3.95 which gives $J_o = 1.5 \times 10^{-2}$ amps $\cdot$ cm^{-2}. η was 6.8 in the theoretical calculations. Since X represents a fraction of carriers, it should be a number less than 1.0. Several reasons are suggested as to why X was greater than 1.0. They are:

(1) The energy gaps were calculated using the formula

$$E_g = 0.181 + (4.52)\ (10^{-4})\ (T) - 0.568x$$

where:

x = mole fraction of SnTe to PbTe

T = temperature in degrees Kelvin

By assuming that both sides are just degenerate such that the fermi level is at the edge of the band means the hole barrier is just equal to the energy gap in the n-type material (the smaller energy gap). The energy gap calculation may be slightly in error.

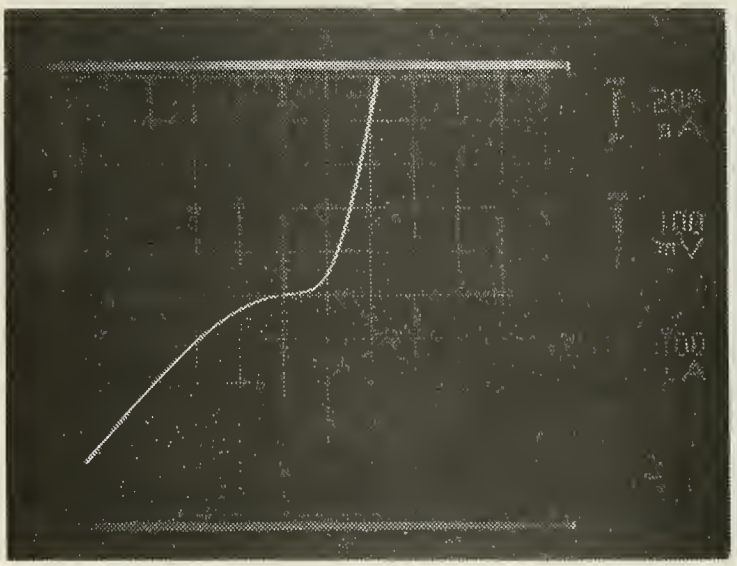

Figure 22. E-Series Typical Diode

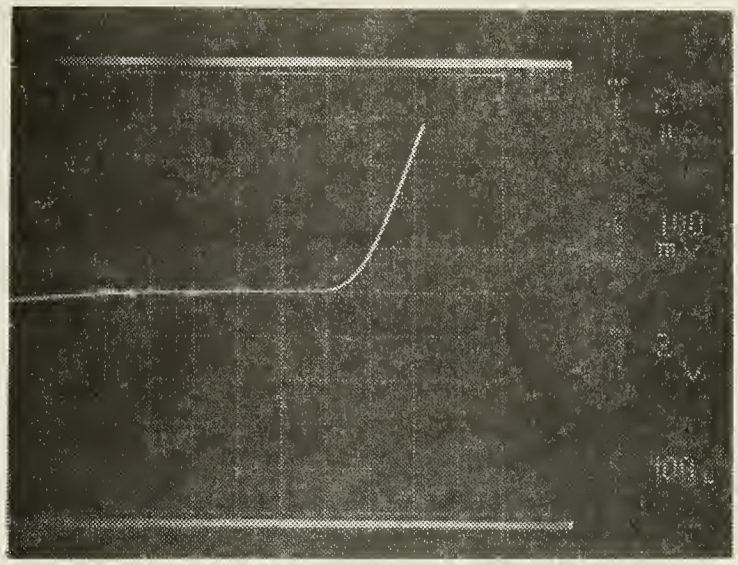

Figure 23. E-Series Best Diode

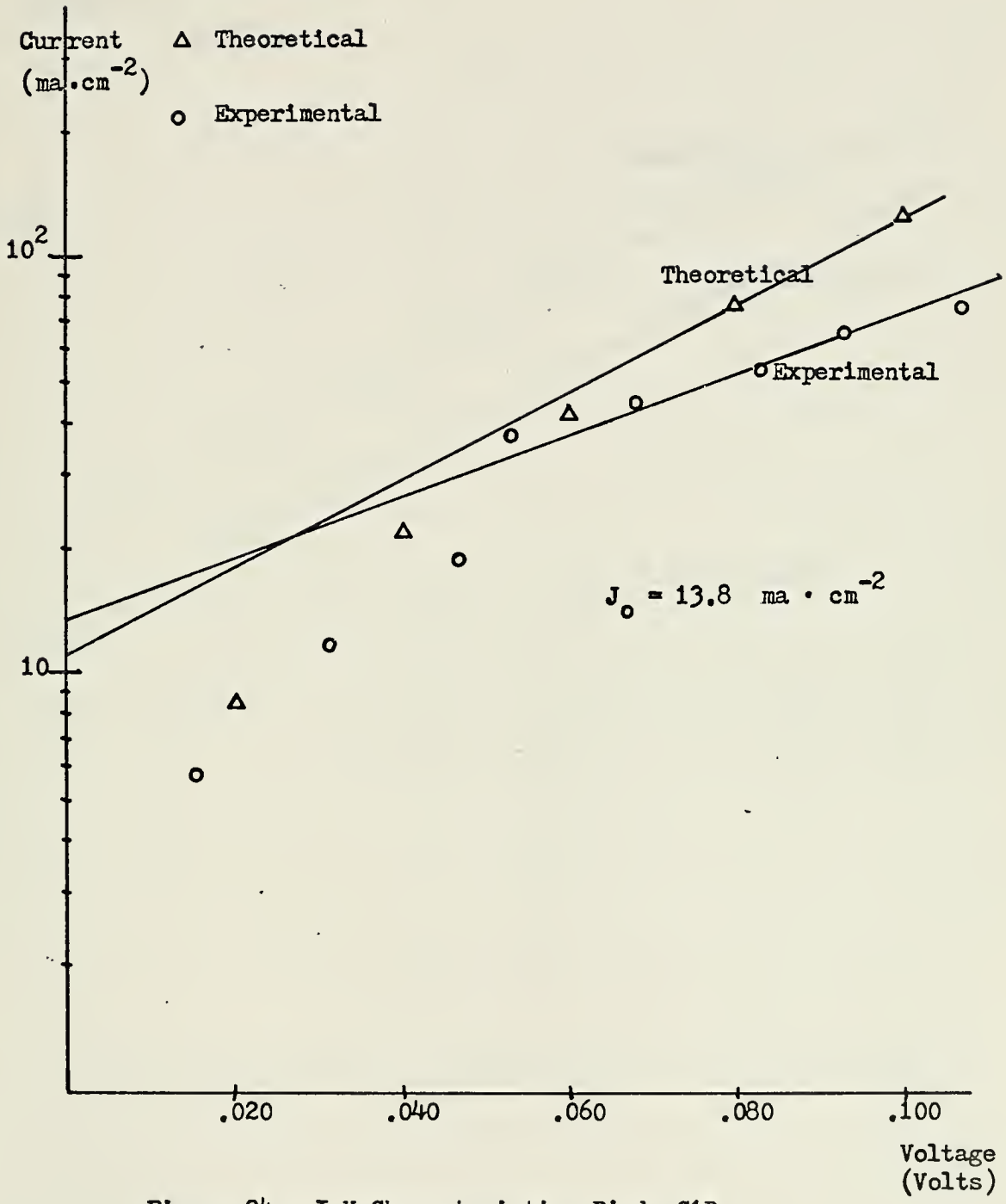

Figure 24. I-V Characteristics Diode C1B

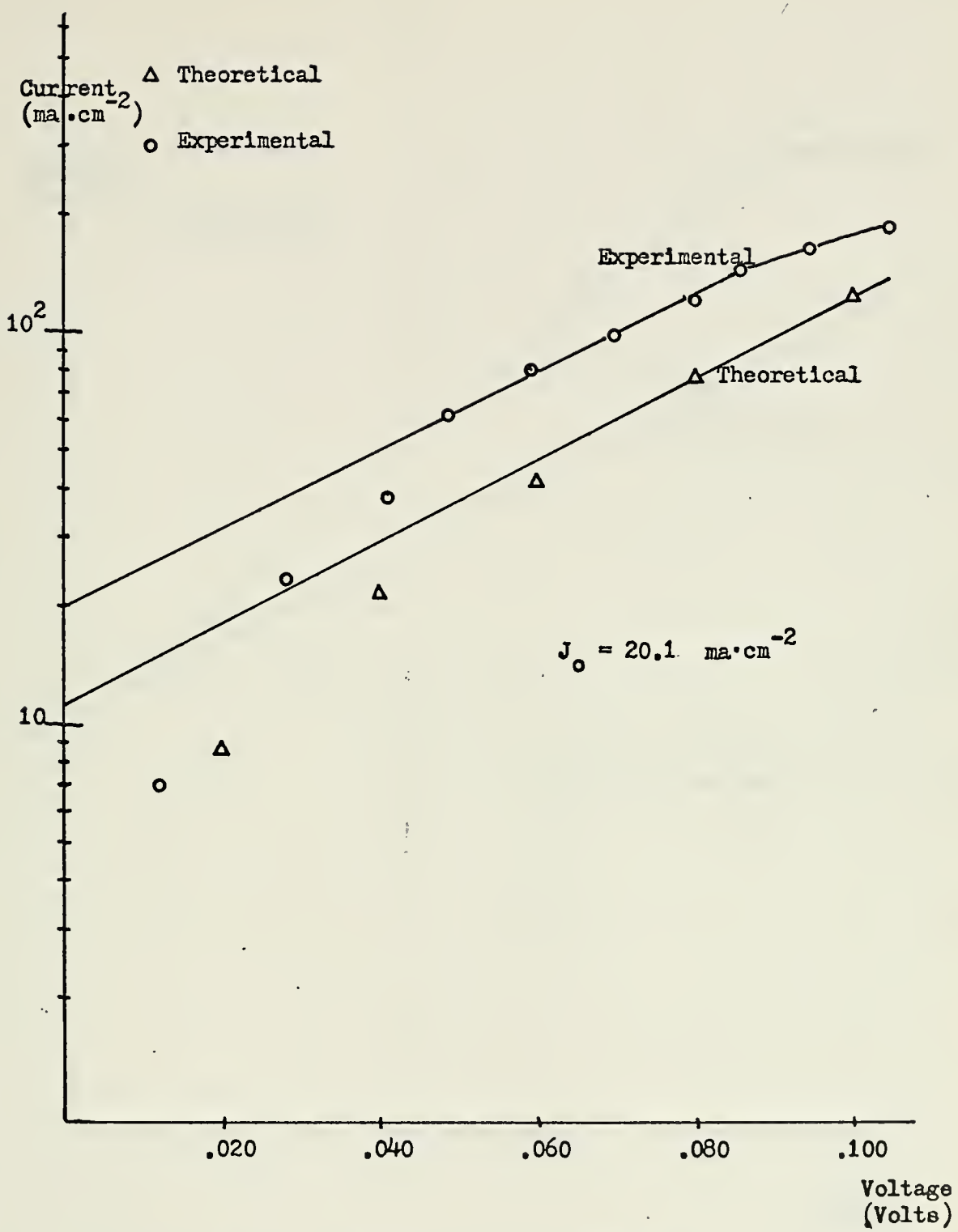

Figure 25. I-V Characteristics Diode C4A

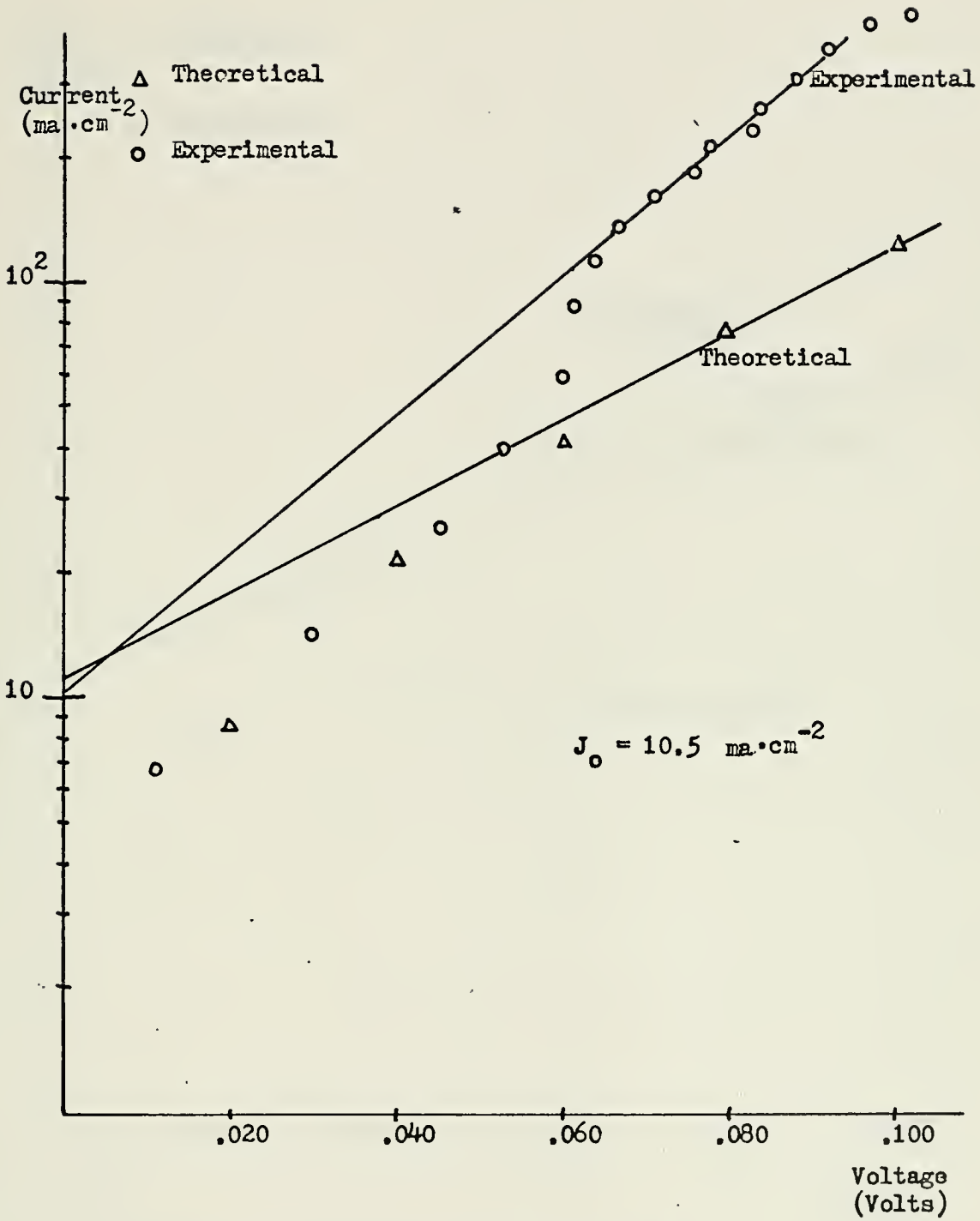

Figure 26. I-V Characteristics Diode C12

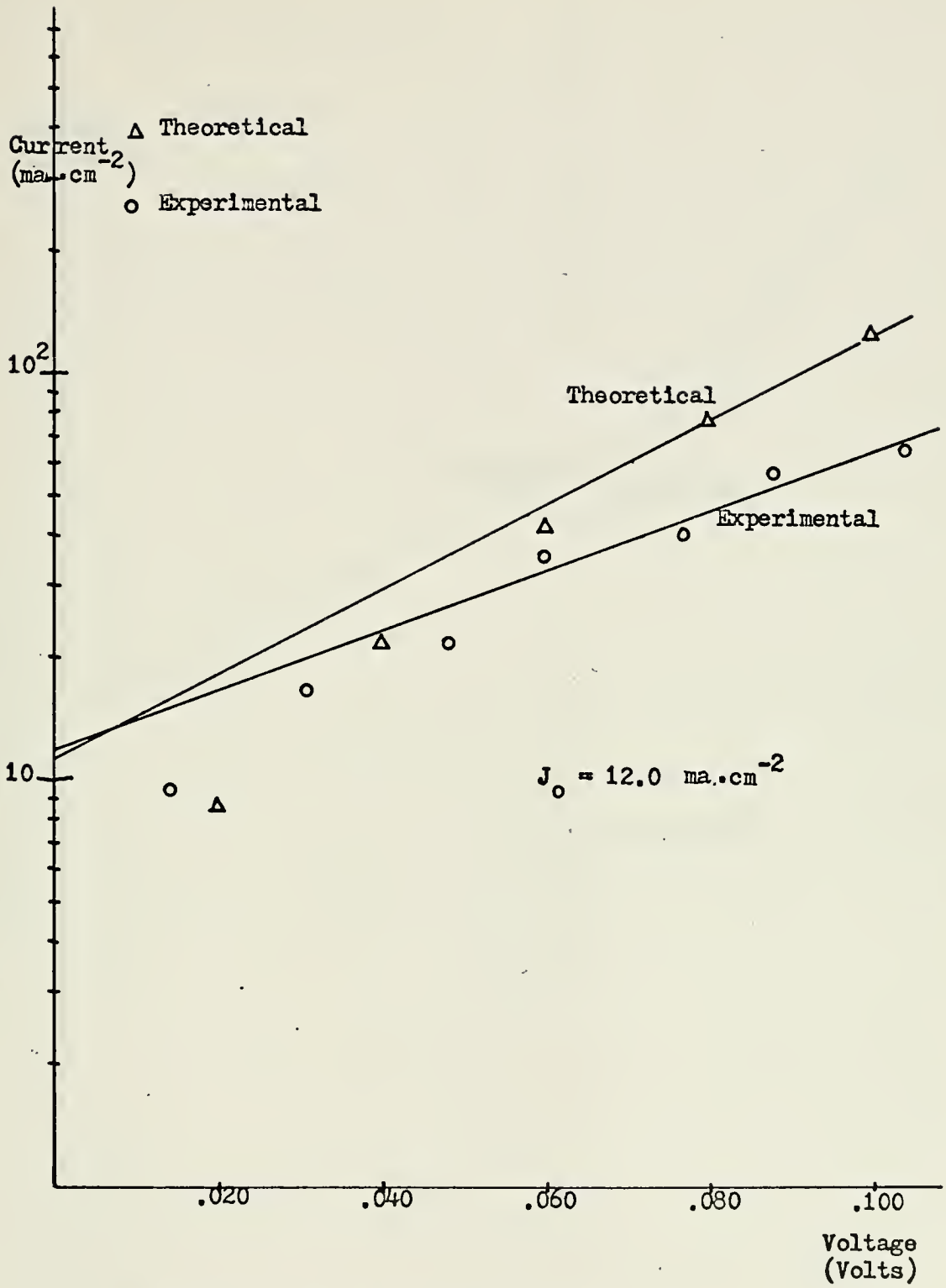

Figure 27. I-V Characteristics Diode E4

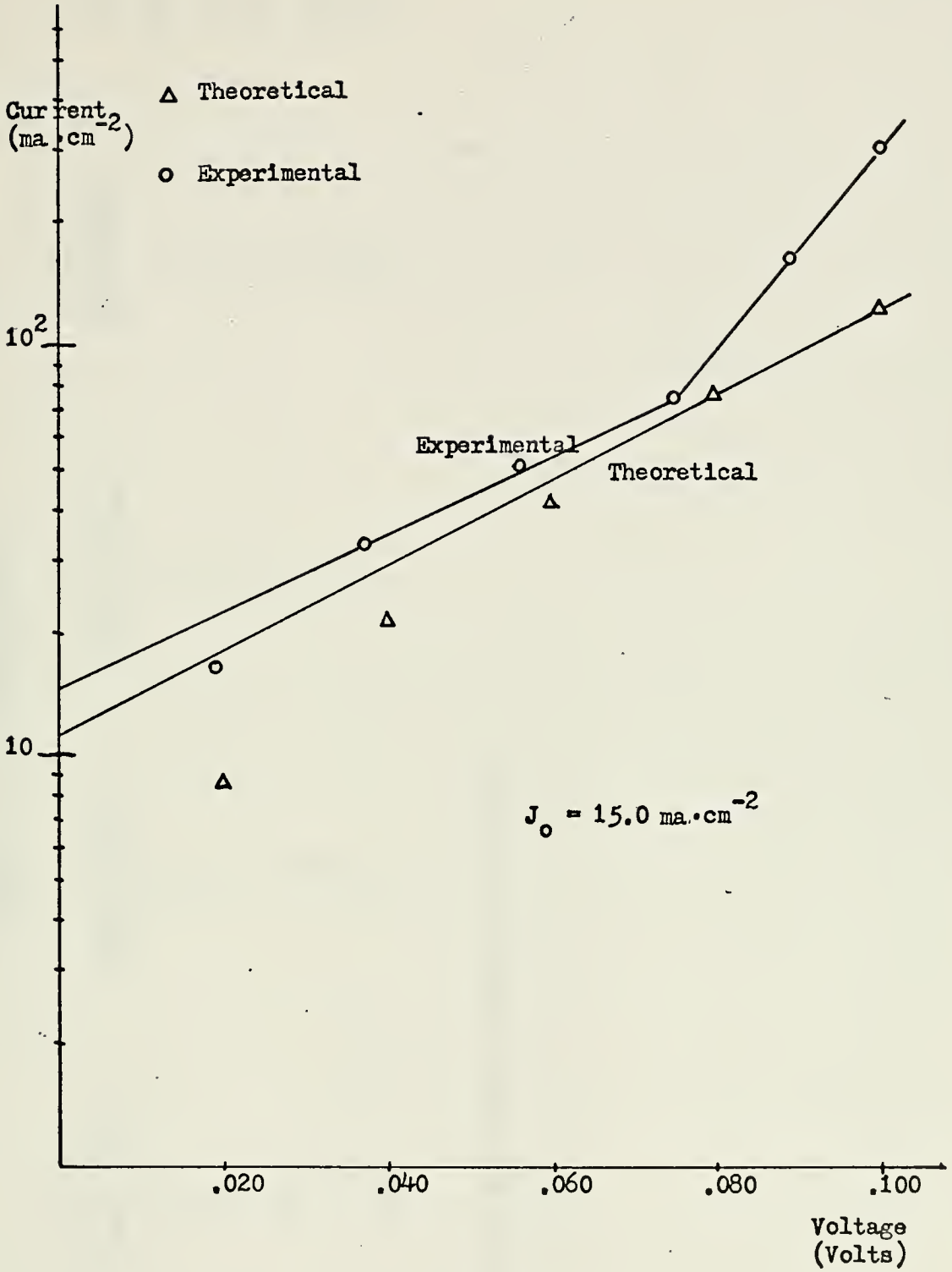

Figure 28. I-V Characteristics Diode E7

TABLE VII

SUMMARY OF I-V CHARACTERISTICS

Diode	J_o ($ma \times cm^{-2}$)	R_o ($ohms \times 10^{-3}$)	A ($cm^2 \times 10^{-3}$)	R_oA ($ohm \times cm^2$)	X
C1B	13.8	1.7	4.3	7.1	3.64
C4A	20.1	2.5	4.3	10.6	5.30
C12	10.5	1.8	4.3	7.7	2.77
E4	15.0	1.7	2.5	3.5	3.17
E7	12.0	3.1	7.0	18.6	3.96

Where X = fraction of carriers crossing the junction

(2) Holes with insufficient energy to cross the barrier may be tunneling across the junction via interface states located in and near the spike in the valence band.

(3) The assumption that the semiconductors are degenerate may be incorrect. However, there is evidence that the semiconductors are indeed degenerate but that the fermi levels instead of being at the respective band edges may even be within the band.

(4) The measured J_o may contain a very large component of current arising from a shunt resistance to the diode. Because all four edges of the diode are cleaved edges, it is very likely that considerable leakage exist along the edge. Additionally, the cleaving steps in the substrates have not been removed. This creates imperfections in the diodes. These two factors may contribute a shunt resistance which greatly increases J_o.

Figures 29 and 30 depict the ln I versus 1/T measured for several diodes at a constant voltage. A straight line plot is shown.

Figures 31 through 33 are linear plots of the forward I-V characteristics of several diodes. The voltage drop across the series resistance has been removed. The theoretical plots are the same values as used in Figures 24 through 28. From these plots V_{BH} was measured. Table VIII summarizes the measured values of V_{BH}.

A theoretical calculation of R_o, the zero bias resistance can be made using the following formula:

$$R_o = \frac{\eta KT}{QI_o}$$

where:

$$I_o = J_o A$$

For a diode of area $5 \times 10^{-3} cm^2$ and using the experimentally measured $J_o = 1.5 \times 10^{-2} amps \cdot cm^{-2}$, gives $R_o = 88.5$ ohms for the ideal diode. The

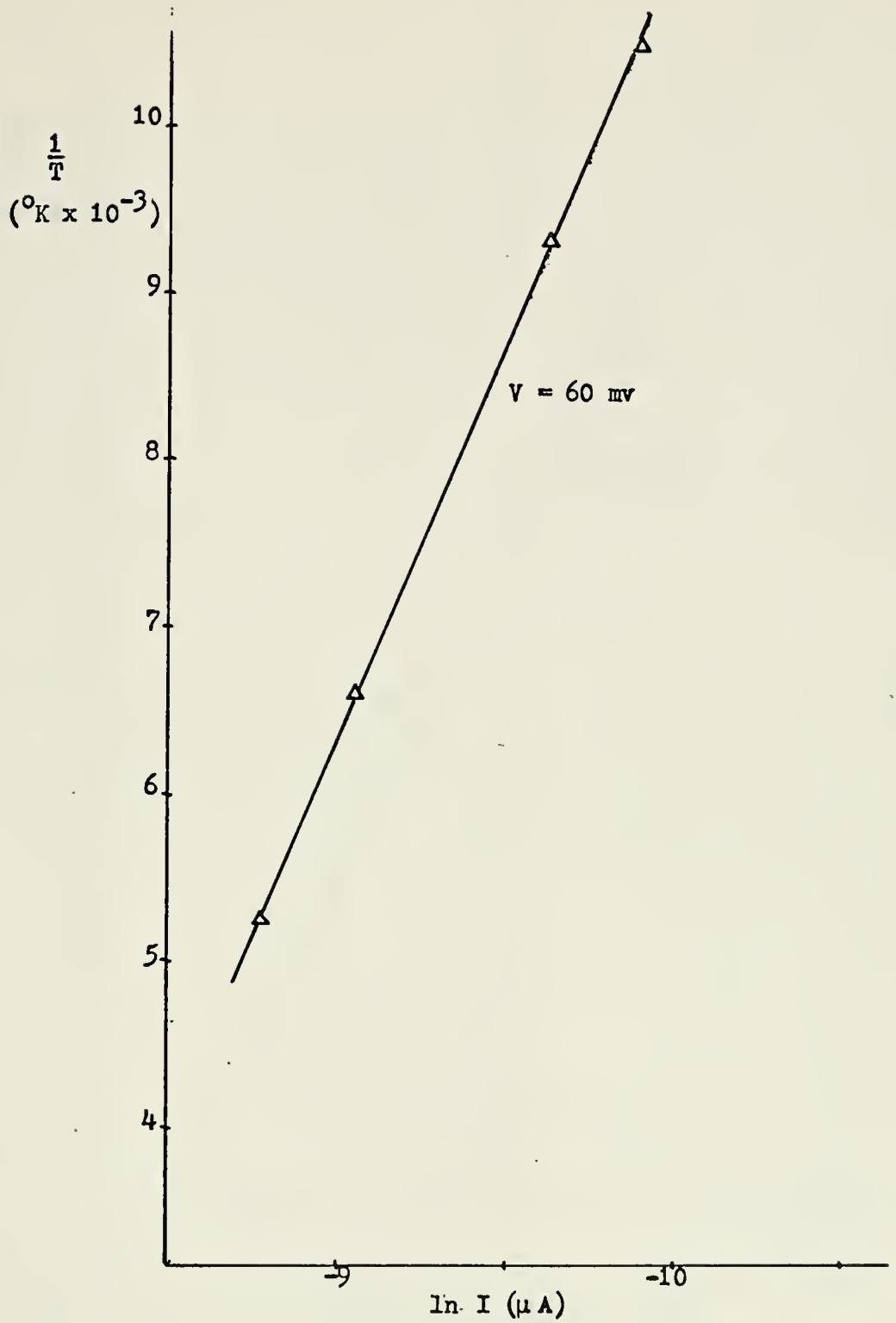

Figure 29. ln I vs 1/T For Diode C-13

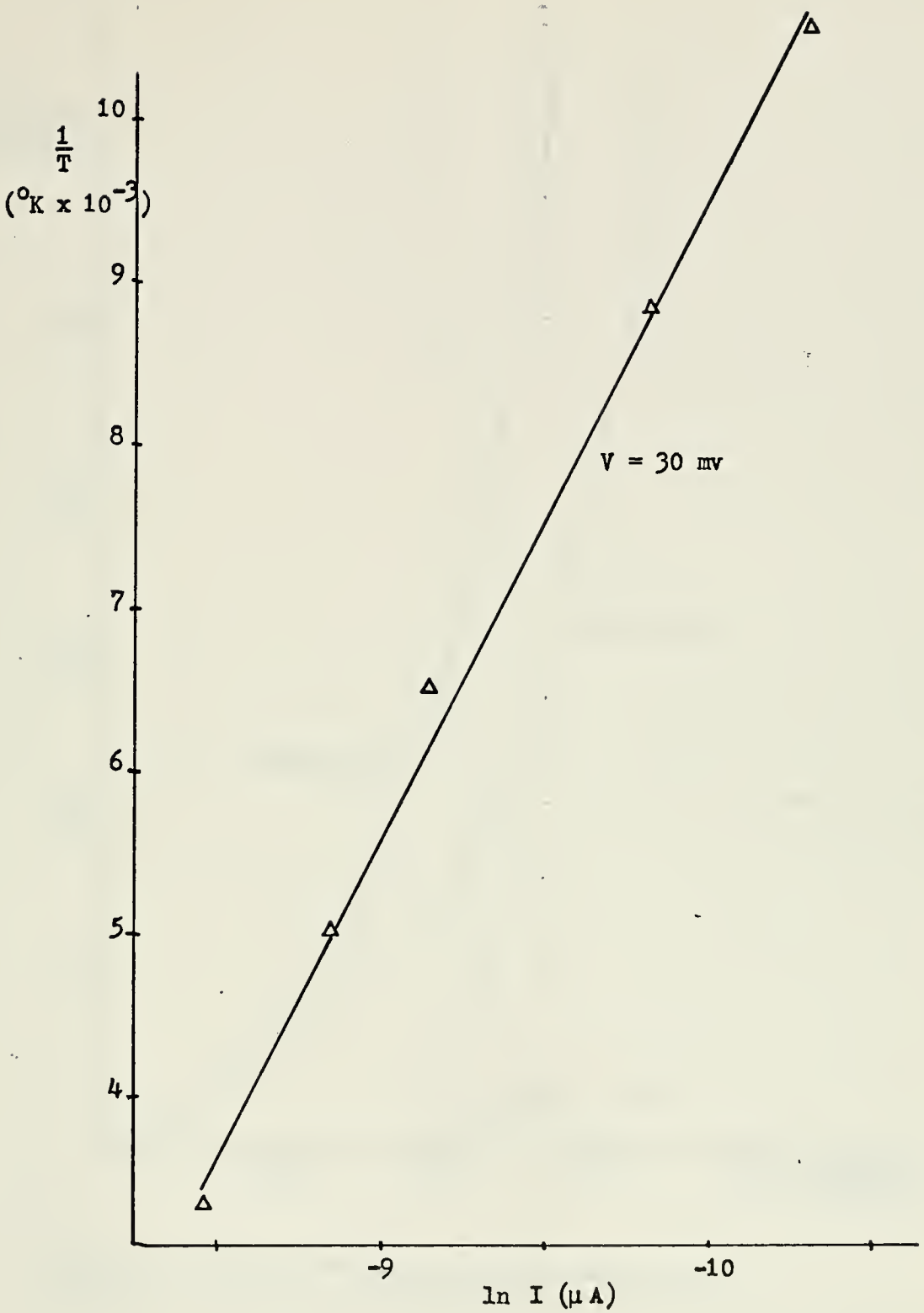

Figure 30. ln I vs 1/T For Diode D-8

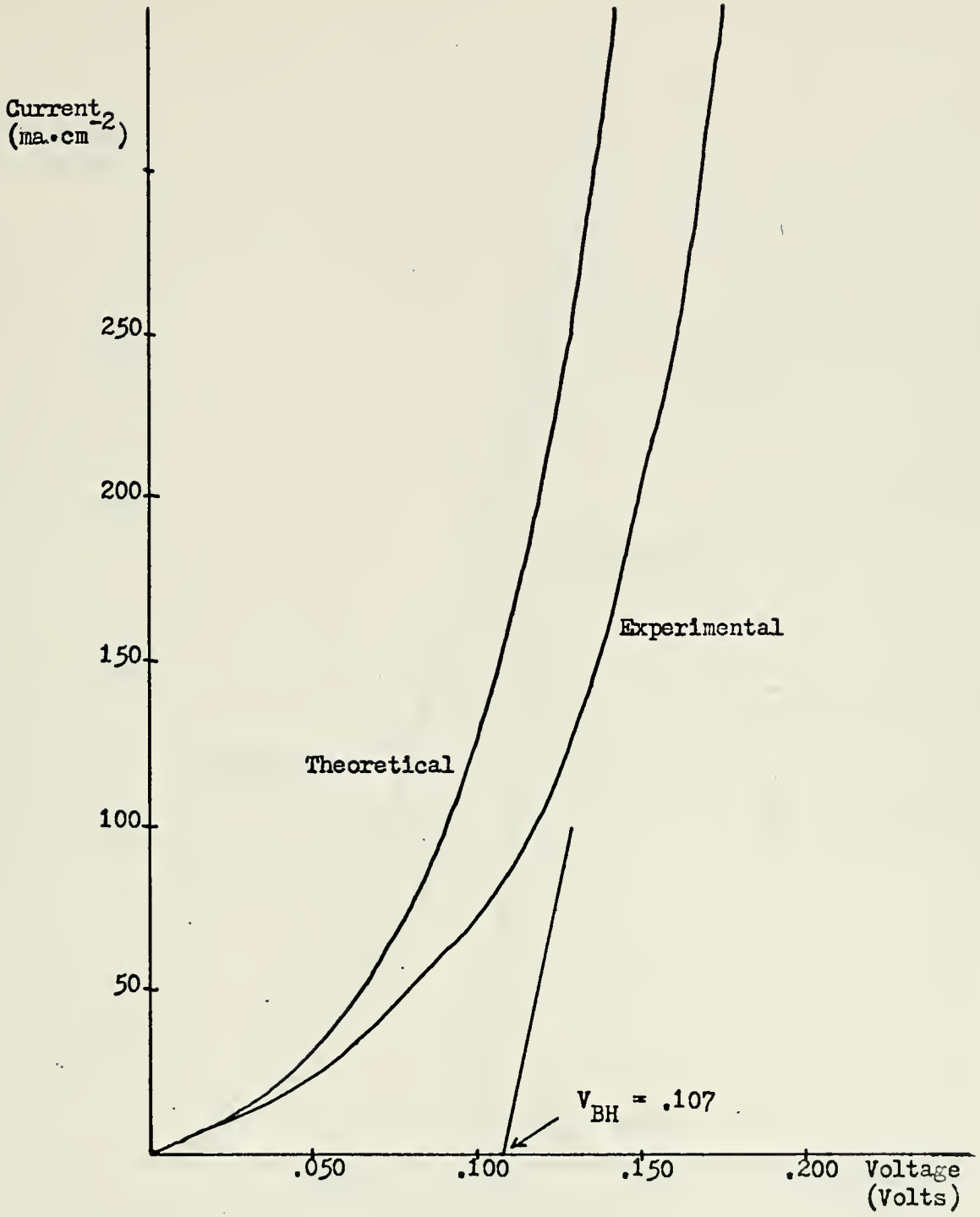

Figure 31. Linear I-V Characteristics Diode C1B

Figure 32. Linear I-V Characteristics Diode C4A

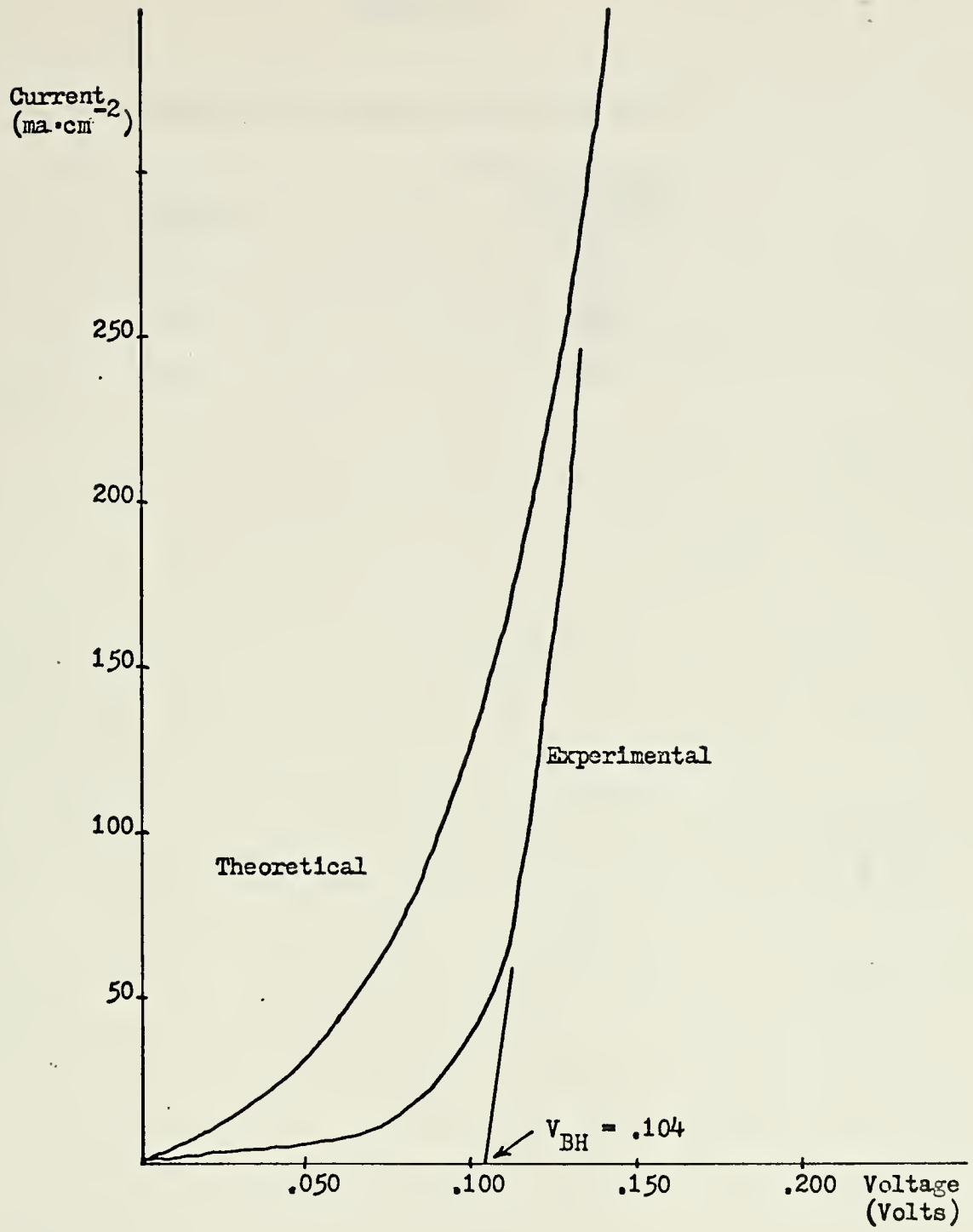

Figure 33. Linear I-V Characteristics For Diode E7

TABLE VIII

SUMMARY OF IV CURVES FROM LINEAR PLOTS

Diode	V_{BH} (volts)
C1B	.107
C4A	.094
E7	.104

R_oA product would be 0.44 ohms $\cdot cm^2$. For a diode with = 6.8, as used in the theoretical analysis, R_o = 602 ohms. The R_oA product in this case would be 3.01 ohms $\cdot cm^2$. From the data presented in Table VII the average R_o = 2160 ohms. For an area of $5 \times 10^{-3} cm^{-2}$ the R_oA product is 10.8 ohms $\cdot cm^2$. If as noted above, the measured value of J_o contains a large component of current arising through the leakage resistance and in fact the actual saturation current is much smaller, then R_o and the R_oA products would be increased.

The I-V analysis has demonstrated a need to improve the quality of the diodes made in order to refine the measured values of J_o, R_o, and V_{BH}. This is necessary to better analyze and compare the experimental results. Two improvements in the fabrication procedures could include etching the diodes and removing the cleavage steps from the KCL substrates.

C. CAPACITANCE-VOLTAGE ANALYSIS

The capacitance-voltage (C-V) measurement has been attempted using a Booton Capacitance Bridge, Model 75D, with a 0.005 volt peak to peak, 1 MHZ, a-c signal. This measurement has failed to produce any meaningful results. The theoretical analysis has indicated that the zero bias capacitance should be about 2×10^6 pf/cm^2. The measured values have been 3 orders of magnitude smaller. As the negative bias was increased, very little change in the capacitance was noted. Also, the d-c bias applied has been damaging to the diodes, creating significant changes in the diode I-V characteristics. The parallel resistance measured has been quite small, on the order of 2-10 k-ohms. As a result of this very low resistance, relatively high currents will flow through the diode at reverse bias conditions. It is felt that the heat generated by this current accounted for the deterioration of the diodes.

The results of the C-V analysis coupled with the seemingly high value of J_o measured in the I-V analysis have indicated the need to improve the quality of the diodes. Three sources of imperfections are felt to be the sources of the trouble. They are: 1) the damage at the edges of the diode created by cleaving the diodes to the desired area, 2) the cleavage steps in the diodes arising from the cleaving of the KCL substrates, and 3) imperfections in the crystal growth, which has been observed under the microscope.

To correct the problems in the diodes, it is proposed that an etching be performed on the diodes. After cleaving the diodes to an area of approximately $1 \times 10^{-2} cm^2$, the surface of the sample should be examined under the microscope to determine the best area. This area should be less than $1 \times 10^{-3} cm^2$. The remainder of the diode can then be etched away. One etching technique that has been recommended by Dr. C. C. Wang, Aerojet Electro Systems Company, is to apply a photoresist to the diode to preserve the desired area and then submit the diode to a hydro-bromic acid etching solution. He has recommended etching to an area of 16 mil^2.

It is hoped that etching could improve the photovoltaic response, reduce J_o, reduce the parallel leakage in the C-V measurement, and provide meaningful results from the C-V analysis.

V. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

N-type thin films can be deposited on cleaved KCL substrates using metal rich $(Pb_{1-x}Sn_x)_yTe$ where y varied between 1.005 and 1.03. The carrier concentration was in the low $10^{17} cm^{-3}$.

N-p heterojunctions displaying good rectification have been made using metal rich source material for the n layer and stiochiometric source material for the p layer. A typical saturation current measured experimentally was 1.5×10^{-2} amps $\cdot cm^{-2}$. R_oA products varied between 3.5 and 18.6 ohm $\cdot cm^2$.

Anderson's Diffusion Model was found to be a good first order approximation for the diode behavior. This was the preferred model. The Thermionic Model was also found to be applicable as an approximation providing an assumption was made that the hole current would dominate. This meant that the hole barrier was used to compute J_o.

The proposed energy band diagram was found to be valid. This model was used to perform the I-V analysis.

Two deposition procedures were used to fabricate the heterojunctions. The multisource procedure was found to be superior to the single source procedure. In the latter method, exposing the interface to the atmosphere seemed to have caused a barrier at the interface.

Photovoltaic response was obtained. Operated at 90^oK, the 500^oK blackbody responsivity up to 0.2 volt $\cdot$ watt^{-1} has been obtained. It was found that the photo responses in diodes with the larger energy gap top layer were more sensitive.

Experimental analysis has indicated the need to improve the quality of the diodes.

B. RECOMMENDATIONS

Future research efforts in the single heterojunction $Pb_{1-x}Sn_xTe$ diodes should include: 1) etching the diodes to remove cleaving damage from the edges and to reduce the diode area, 2) spectral response analysis should be performed to further verify the junction behavior, 3) C-V analysis should be conducted to support the I-V analysis, 4) polishing the KCL substrates to remove the cleaving steps, 5) investigation of different contacts to the p and n layers, and 6) more accurate measurement of the thickness of each layer using a scanning electron microscope.

Other heterojunction research should include: 1) making of n^+ source material, with carrier concentration in the $10^{18} cm^{-3}$ range, to be used in double heterojunctions, 2) investigations of the double heterojunction, probably $p\text{-}n\text{-}n^+$, 3) investigate the Schottky barriers to determine the semiconductor surface properties, 4) investigate heterojunctions made from PbSnSe, 5) investigate luminence of heterojunctions, and 6) investigation of lasing from these heterojunctions.

```
C
C   PROGRAM TO ANALYZE C-V CHARACTERISTICS OF PBSNTE DIODES.
C
C
C   THEORETICAL ANALYSIS BASED ON ANDERSONS MODEL.  EQUATIONS SOLVED ARE
C
C     C=SQRT(Q*N*E/4*(VD-V))
C
C   WHERE     C=CAPACITANCE IN PF/SQCM          Q=ELECTRON CHARGE
C             N=CARRIER CONC                    E=DIELECTRIC CONSTANT
C             VD=BARRIER VOLT                   V=APPLIED VOLTAGE
C
C
C   ASSUMPTIONS
C        1. CARRIER CONC SAME ON BOTH SIDES
C        2. DIELECTRIC CONSTANT SAME ON BOTH SIDES
C        3. INTERFACE STATE DENSITY SMALL
C        4. BARRIER VOLT = 0.136
C
C
C   PROGRAM VARIABLES
C    VO,TC - THEORITECAL VOLTAGE AND CAPACITANCE
C    TCC - THEORITICAL 1/SQCAP
C    DV,DC - DIODE VOLTAGE AND CAPACITANCE
C    DCC - 1/SQCAP  FOR DIODE
C
C
C   INPUT DATA FORMAT
C
C    FIRST CARD-NUMBER OF DIODES TO BE ANALYZED  FORMAT I2 (NOTE. ONE
C    GRAPH IS PLOTTED FOR EACH DIODE AND ONLY FIVE MAY BE PLOTTED)
C
C    SECOND CARD-DIODE DESIG  FORMAT A4
C
C    THIRD CARD-NUMBER OF DATA POINTS  FORMAT I2
C
C    FOURTH CARD-DIODE AREA IN SQCM  FORMAT E9.3
C
C    FIFTH CARD-DATA POINTS BETWEEN WHICH SLOPE IS COMPUTED  FORMAT 2I2
C   (NOTE. UPPER LIMIT FIRST.  SLOPE USED TO COMPUTE CARRIER CONC.)
C
C    SIXTH CARDS-DIODE DATA POINTS  FORMAT 2E9.3 (NOTE.VOLTAGE FIRST
C    IN VOLTS THEN CAP IN PF. NUMBER DATA POINTS SHOULD EQUAL NUMBER
C    SPECIFIED ON THIRD CARD.)
C
```

```
C    THEN START WITH SECOND CARD FOR NEXT DIODE
C
C
C    VALUES FOR THEORETICAL ANALYSIS IS ESTABLISHEC IN DATA STATEMENTS
C    AND AT THE BEGINNING OF THE PROGRAM.  VARIABLES ARE
C
C    Q=Q  DATA STATEMENT
C    ES=DIELECTRIC CONSTANT=400*8.854E-14
C    VB=VD  ASSUMED EQUAL TO 0.136 EV
C    CO=N  ASSUMED 3.0E 17
C
C
C
C   OUTPUT IS IN VOLTS AND PF/SQCM.  A GRAPH OF 1/SQCAP IS PLOTTED
C    FOR EACH DIODE.  NO THEORETICAL PLOTS ARE MADE.
C   GRAPHS ARE MADE FOR ONLY THE FIRST FIVE DIODES ANALIZED.
C
C
C
C
C
C
C           PROGRAM
C
C
      DIMENSION VO(30),TC(30),TCC(30),DC(30),DCC(30),DV(30)
      REAL*8 TITLE(12)/'SMI22254',' PBSNTE ','DICDE AN','ALYSIS  ','  DI
     1ODE ','        ','X-AXIS=V','OLTS    ','Y-AXIS=P','F/SQCM  ',
     2'JUNE 73 ','RESEARCH'/
      REAL*8 NAME(12)/'SMI22254',' PBSNTE ','DIODE AN','ALYSIS  ',
     1'  DIODE ','        ','X-AXIS=V','OLTS Y-A','XIS=1/CS','QUARED  ',
     2'BARVOLT=','        '/
      REAL LABT/'THRY'/
      REAL LABE/'EXPT'/
      DATA Q/1.6E-19/,EA/8.854E-14/,EE/1.0E 24/,EF/1.0E-12/
      VB=0.136
      ES=400.0*EA
      CO=3.0E 17
      VO(1)=0.0
      DO 1000 I=2,30
      M=I-1
      VO(I)=VO(M)-0.025
 1000 CONTINUE
      WRITE(6,7000)
      WRITE(6,7004)VB,CO
      WRITE(6,7005)
      WRITE(6,7006)
      DO 1500 I=1,30
```

```
      CA=((Q*CO*ES)/(4.0*(VB-VO(I))))*EE
      TCC(I)=1.0/CA
      TC(I)=SQRT(CA)
      WRITE(6,7001)VO(I),TC(I)
 1500 CONTINUE
      READ(5,6000)K
      DO 3000 I=1,K
      READ(5,6001)DIODE
      READ(5,6000)N
      READ(5,6002)AREA
      READ(5,6003)LU,LL
      WRITE(6,7011)DIODE
      WRITE(6,7012)N,AREA,LU,LL
      WRITE(6,7013)
      DO 2000 J=1,N
      READ(5,6004)DV(J),DC(J)
      DV(J)=-DV(J)
      WRITE(6,7014)DV(J),DC(J)
      DC(J)=DC(J)*EF/AREA
      DCC(J)=1.0/DC(J)**2
 2000 CONTINUE
      SL=(DCC(LU)-DCC(LL))/(DV(LU)-DV(LL))
      CACON=(4.0/(Q*ES*SL))
      WRITE(6,7002)DIODE
      WRITE(6,7007)CACON,DV(LU),DV(LL)
      WRITE(6,7009)
      WRITE(6,7010)
      DO 2500 NU=1,N
      DC(NU)=DC(NU)/EF
      WRITE(6,7003)DV(NU),DC(NU),DCC(NU)
 2500 CONTINUE
      IF(I.GT.5) GO TO 3000
      NAME(6)=DIODE
      CALL DRAW(N,DV,DCC,0,0,LABE,NAME,0.1,0.0,0,6,0,2,8,8,1,LAST)
 3000 CONTINUE
 6000 FORMAT(I2)
 6001 FORMAT(A4)
 6002 FORMAT(E9.3)
 6003 FORMAT(2I2)
 6004 FORMAT(2E9.3)
 7000 FORMAT('1','THEORETICAL C-V ANALYSIS PBSNTE DIODES',//)
 7001 FORMAT(' ',2E15.3)
 7002 FORMAT('1','EXPERIMENTAL DIODE C-V ANALYSIS. DIODE',1X,A4,//)
 7003 FORMAT(' ',3E15.3)
 7004 FORMAT(' ','BARRIER VOLTAGE = ',F5.3,5X,'CARRIER CONCENTRATION = '
     1,E9.3,//)
 7005 FORMAT(' ',7X,'VOLTAGE',6X,'CAPACITANCE')
 7006 FORMAT(' ',7X,'(VOLTS)',9X,'(PF)')
```

```
7007 FORMAT(' ','CARRIER CONCENTRATION =',1X,E9.3,2X,'COMPUTED BETWEEN',1X
    1,1X,E9.3,1X,'VOLTS AND',1X,E9.3,1X,'VOLTS')
7009 FORMAT(' ',6X,'VOLTAGE',6X,'CAPACITANCE',2X,'1/CAP SQUARED')
7010 FORMAT(' ',6X,'(VOLTS)',7X,'(PF/SQCM)')
7011 FORMAT('1','INPUT DATA DIODE',A4)
7012 FORMAT(' ','N=',I2,5X,'AREA=',E9.3,5X,'LU=',I2,2X,'LL=',I2)
7013 FORMAT(' ','VOLTAGE',2X,'CAPACITANCE')
7014 FORMAT(' ',2E9.3)
     STOP
     END
```

```
C
C   PROGRAM TO ANALYZE I-V CHARACTERISTICS OF PBSNTE DIODES.
C
C
C   THEORETICAL ANALYSIS BASED ON ANDERSONS DIFFUSION MODEL.
C   EQUATIONS SOLVED ARE
C
C    J=JC*(EXP(Q*V/N*K*T)-U)
C
C    JO IS THE SATURATION CURRENT READ IN ON A DATA CARD
C
C    WHERE    J=CURRENT DENSITY IN MA/SQCM      V=APPLIED VOLTAGE
C             Q=ELECTRON CHARGE                 N=DEVIATION FROM IDEAL
C             K=BOLTZ. CONSTANT                 T=TEMPERATURE IN K
C
C
C    PROGRAM VARIABLES ARE DEFINED-
C       T=T  INITIALIZED IN DATA STATEMENT (IIDS)
C       Q=Q  IIDS
C        B=K  IIDS
C       A=N  IIDS
C       TC,TV THEORETICAL CURRENT AND VOLTAGE
C       V=V
C       K=NUMBER OF DIODES ANALIZED
C       DIODE=DESIGNATION OF DIODE
C       N=NUMBER OF DIODE DATA POINTS
C       AREA=DIODE AREA IN SQCM
C       LU AND LL= POINTS BETWEEN WHICH RSER COMPUTED
C       AV=ACTUAL DIODE VOLTAGE
C       AC=ACTUAL DIODE CURRENT
C       CR=AMOUNT OF AV ACROSS RSER
C       CD=DIODE VOLTAGE WITH CR REMOVED FROM AV
C       RSER=DIODE SERIES RESISTANCE
C
C
C    MATRICES ARE DIMENSIONED TO 150.  VALUES FOR N ARE LOADED INTO
C   A MATRIX (A) AND CAN BE VARIED.  THE A MATRIX IS ALSO
C   DIMENSIONED TO 150 TO PERMIT SELECTING A DIFFERENT N VALUE
C   FOR EACH VOLTAGE POINT.  WHEN CHANGING N IT WILL RESULT IN
C   A SMOOTHER PLOT IF N IS CHANGED SLOWLY OVER SEVERAL DATA POINTS.
C   JO, THE SATURATION CURRENT MUST BE READ IN ON A DATA CARD
C   APPEARING AT THE BEGINNING OF THE PROGRAM.  THERE IS NO PROVISION
C   TO CHANGE N FOR DIFFERENT DIODES.
C
```

```
C
C   INPUT DATA FORMAT (ALL DATA STARTS IN COLUMN 1, ALL DATA FIELDS MUST
C   BE RIGHT ADJUSTED BY USER.  NO DATA CARDS ARE NEEDED FOR THEORETICAL
C   ANALYSIS.)
C
C   FIRST CARD- NUMBER OF DIODES TO BE ANALIZED  FORMAT I3  (NOTE.
C   ONLY FIVE GRAPHS CAN BE PLOTTED AND ONE GRAPH IS PLOTTED FOR
C   EACH DIODE)
C
C   SECOND CARD-DIODE DESIGNATION  FORMAT A4
C
C   THIRD CARD- NUMBER OF DIODE DATA POINTS- FORMAT I3
C
C   FOURTH CARD- DIODE AREA IN SQCM  FORMAT E9.3
C
C   FIFTH CARD- DATA POINTS BETWEEN WHICH RSER IS COMPUTED  FORMAT 2I2
C   (NOTE.UPPER LIMIT FIRST)
C
C   SIXTH CARDS- DIODE DATA POINTS- FORMAT 2E9.3  (NOTE, CURRENT FIRST IN
C   AMPS/SQCM THEN VOLTAGE IN VOLTS. NUMBER OF DATA CARDS MUST EQUAL
C   NUMBER SPECIFIED ON THIRD CARD.)
C
C   THEN CONTINUE WITH NEXT DIODE STARTING WITH SECOND CARD
C   NUMBER DIODES SHOULD EQUAL NUMBER ON CARD ONE
C
C   OUTPUT DATA IS GIVEN IN VOLTS AND MA/SQCM. GRAPHS ARE 8 BY 8
C
C   GRAPHS ARE PLOTTED FOR ONLY THE FIRST FIVE DICDES ANALYZED.
C
C   RSER COMPUTED FROM SLOPE BETWEEN DATA POINTS ON CARD FIVE IS
C   REDUCED BY 85%.
C
C
C
C
C                   PROGRAM
C
      DIMENSION TC(150),TV(150),AC(150),AV(150),CD(150),CR(150),A(150)
      REAL THRY/'THRY'/
      REAL EXPT/'EPPT'/
      REAL CORR/'CORR'/
      REAL*8 TITLE(12)/'SMI12254',' PBSNTE ','DIODE AN','ALYSIS  ',
     1'   DIODE','        ','X-AXIS=V','OLTS    ','Y-AXIS=M','A/SQCM  '
     2,'JUNE 73 ','RESEARCH'/
```

```
      DATA TAU/1.0E-09/,DP/66.4/,VDP/.103/,X/3.96/,T/77.0/,PN/5.0E 17/,
     1UH/.10E 05/
      DATA A/150*6.8/
      DATA CO/0.150E-01/
      DATA T/77.0/
      DATA Q/1.6E-19/,B/1.38E-23/
      TC(1)=0.0
      TV(1)=0.0
      V=0.001
      L=2
 1000 C=CO*(EXP((Q*V)/(A(L)*B*T))-1.0)
      TC(L)=C*1000.0
      TV(L)=V
      V=V+0.001
      L=L+1
      IF(L.LT.151) GO TO 1000
      WRITE(6,7000)
      WRITE(6,7001)
      WRITE(6,7002) TAU,DP,VDP
      WRITE(6,7003)X,T,PN
      WRITE(6,7004)UH,CO
      WRITE(6,7005)
      WRITE(6,7006)
      DO 1400 K=1,150
      WRITE(6,7007)TC(K),TV(K),A(K)
 1400 CONTINUE
      READ(5,6000)K
      DO 3000 M=1,K
      READ(5,6004)DIODE
      READ(5,6000)N
      READ(5,6003)AREA
      READ(5,6005)LU,LL
      AC(1)=0.0
      AV(1)=0.0
      CD(1)=0.0
      CR(1)=0.0
      WRITE(6,7012)DIODE
      WRITE(6,7008)
      N=N+1
      DO 2000 I=2,N
      READ(5,6001)AC(I),AV(I)
      WRITE(6,7009)AC(I),AV(I)
 2000 CONTINUE
      RSER=(AV(LU)-AV(LL))/(AC(LU)-AC(LL))*0.85
      WRITE(6,7011)DIODE
      WRITE(6,7010)RSER,AV(LU),AV(LL)
      WRITE(6,7013)
      WRITE(6,7014)
```

```
      DO 2500 I=1,N
      CR(I)=AC(I)*RSER
      CD(I)=AV(I)-CR(I)
      AC(I)=(AC(I)/AREA)*1000.0
      WRITE(6,7015)AC(I),AV(I),CD(I),CR(I)
2500  CONTINUE
      IF(M.GT.5) GO TO 3000
      TITLE(6)=DIODE
      CALL DRAW(145,TV,TC,1,0,THRY,TITLE,.05,0.0,0,0,0,0,8,8,1,LAST)
      CALL DRAW(N,AV,AC,2,0,EXPT,TITLE,.05,0.0,0,0,0,0,8,8,1,LAST)
      CALL DRAW(N,CD,AC,3,0,CORR,TITLE,.05,0.0,C,0,0,0,8,8,1,LAST)
3000  CONTINUE
6000  FORMAT(I3)
6001  FORMAT(2E9.3)
6002  FORMAT(F4.2)
6003  FORMAT(E9.3)
6004  FORMAT(A4)
6005  FORMAT(2I2)
7000  FORMAT('1','THEORETICAL ANALYSIS PBSNTE DIODES USING ANDERSON DIFF
     1USION MODEL',//)
7001  FORMAT(' ','PARAMETERS.')
7002  FORMAT(' ','LIFETIME = ',E9.3,/,' ','DIFFUSION CONSTANT = ',E9.3,/
     1,' ','BARRIER VOLTAGE FOR HOLES = ',E9.3)
7003  FORMAT(' ','FRACTION OF CARRIERS WITH SUFF. ENERGY WHICH ACTUALLY
     1DO CROSS THE BARRIER = ',E9.3,/,' ','TEMPERATURE = ',E9.3,/,' ','H
     2OLE CONCENTRATION ON P-SIDE = ',E9.3)
7004  FORMAT(' ','HOLE MOBILITY = ',E9.3,/,' ','SATURATION CURRENT = ',E
     19.3,2X,'AMPS',//)
7005  FORMAT(' ','ASSUMPTIONS.',/,' ','1. ANDERSONS MODEL APPLIES WITH H
     1OLE CURRENT DOMINATING.',/,' ','I. CONDUCTION BAND AND VALENCE BAN
     2D DISCONTINUNITIES ARE EQUAL.',/,' ','3. BARRIER VOLTAGE = 0.16 EV'
     3',/,' ','4. DEGENERATE SEMICONDUCTOR.',/,' ','5. NONDEGENERATE DIF
     4FUSION CONSTANT AND HALL MOBILITY USED.',//)
7006  FORMAT(' ',6X,'CURRENT',8X,'VOLTAGE',8X,'N',/,' ',6X,'(MA/SQCM)',
     16X,'(VOLTS)')
7007  FORMAT(' ',2E15.3,4X,F4.2)
7008  FORMAT(' ',7X,'CURRENT',8X,'VOLTAGE')
7009  FORMAT(' ',2E15.3)
7010  FORMAT(' ','DIODE SERIES RESISTANCE =',F8.2,'OHMS',4X,'COMPUTED
     1BETWEEN',E9.3,'VOLTS AND',E9.3,'VOLTS',//)
7011  FORMAT('1','EXPERIMENTAL DIODE IV ANALYSIS DIODE',1X,A4,/,/)
7012  FORMAT('1','INPUT DATA - DIODE',1X,A4,/,/)
7013  FORMAT(' ',6X,'CURRENT',8X,'TOTALVOLT',6X,'DIODEVOLT',6X,'RESISTVO
     1LT')
7014  FORMAT(' ',5X,'(MA/SQCM)',7X,'(VOLTS)',8X,'(VOLTS)',8X,'(VOLTS)',
     1/,/)
7015  FORMAT(' ',4E15.3)
8000  FORMAT(' ',E15.3)
```

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ABSTRACT

The electrical and photovoltaic properties of single heterojunction (SH) $Pb_{1-x}Sn_xTe$ diodes have been studied. SH diodes were fabricated by sequential depositions of p-type $Pb_{0.86}Sn_{0.14}Te$ using stiochiometric source material and n-type $Pb_{0.80}Sn_{0.20}Te$ using metal rich source material. At T = 77°K, their energy gaps are 0.136 ev and 0.103 ev, respectively. SH diodes of good rectification with R_oA products ranging from 3.5 to 18.6 have been obtained. Operated at 100°K, 500°K blackbody photovoltaic responses up to 0.2 volt/watt has been obtained.

The current-voltage characteristics have been studied theoretically based on both the Anderson Diffusion Model and the Thermionic Emission Model. Using Anderson's model, and assuming E_c = 0, constant electron affinity across the junction, fair agreements have been found between measurements and theoretical calculations.

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